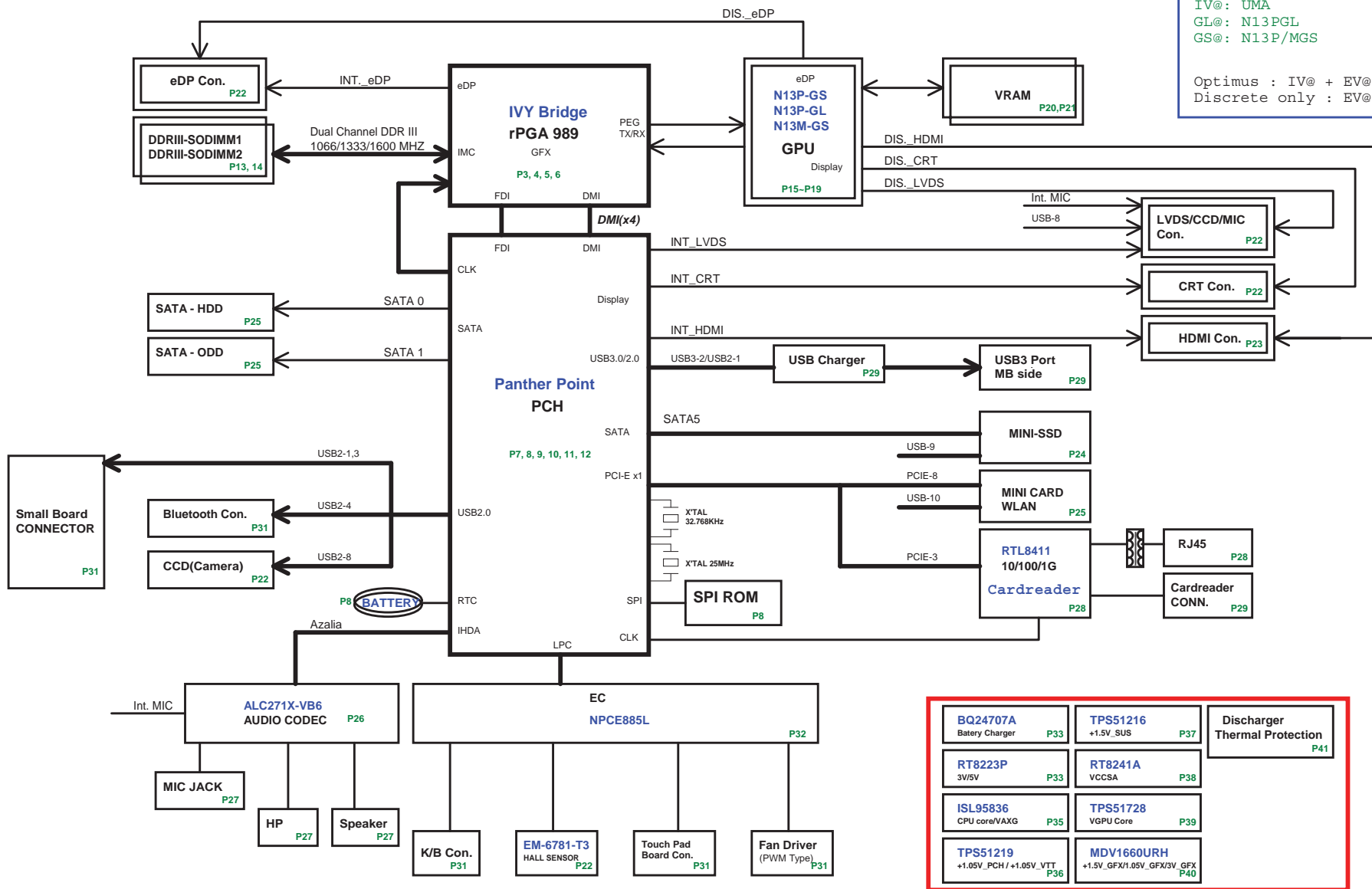


ZQTA/ZQSA CRV SYSTEM BLOCK DIAGRAM

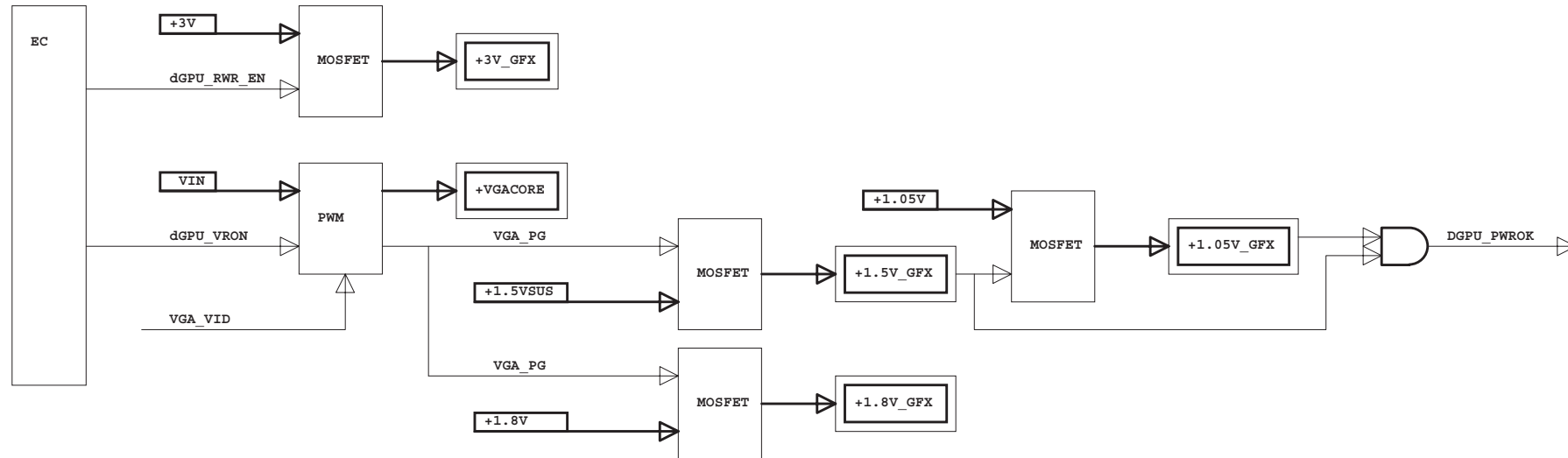
BOM

IV@ : iGPU
 EV@ : dGPU
 OP@ : Optimus
 DO@ : Discrete only
 SP@ : Special
 SNP@ : N13PGS/GL
 IV@ : UMA
 GL@ : N13PGL
 GS@ : N13P/MGS

Optimus : IV@ + EV@ + OP@
 Discrete only : EV@ + DO@



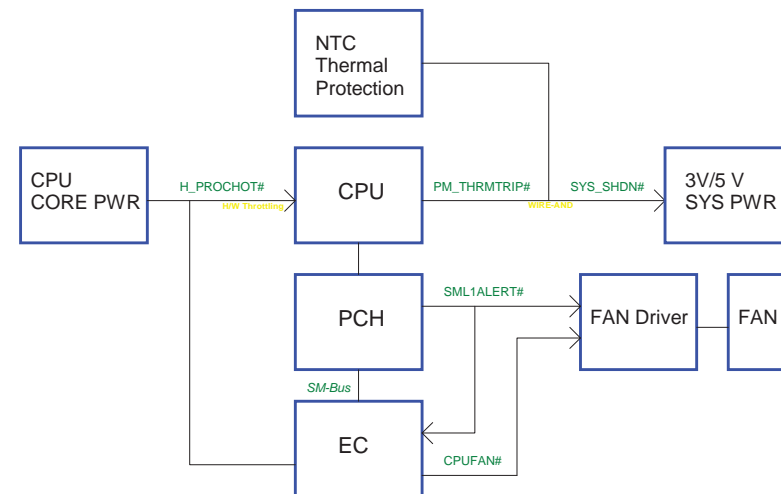
VGA power up sequence



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	VRON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER/IVY/SNB bridge VCCIO	MAINON	S0
+VCCSA	+0.9V	CPU POWER	HWPG_VTT	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
			MAINON	S0

Thermal Follow Chart



IVY Bridge Processor (CLK,MISC,JTAG)



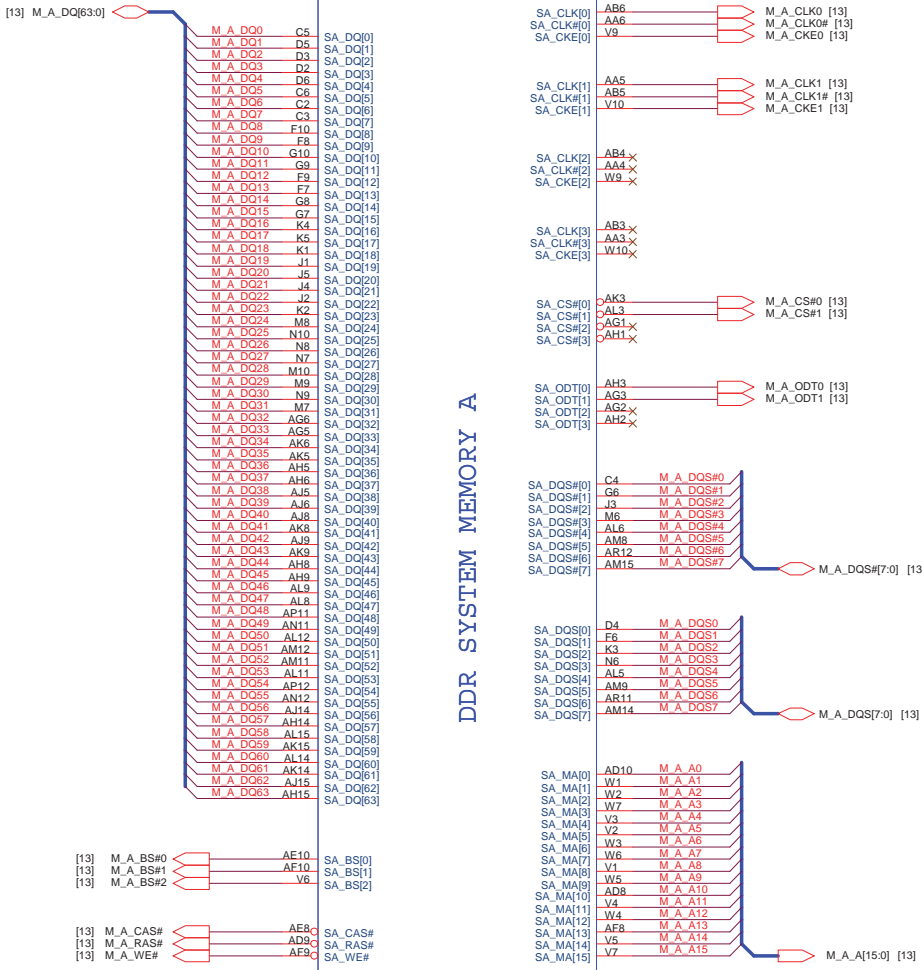
1

IVY Bridge Processor (DDR3)

U16C

Ivy Bridge_rPGA_2DPC_Rev0p61

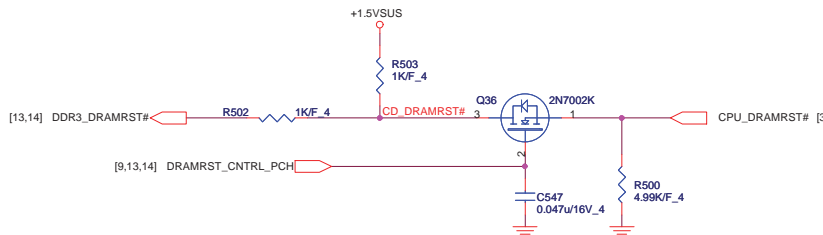
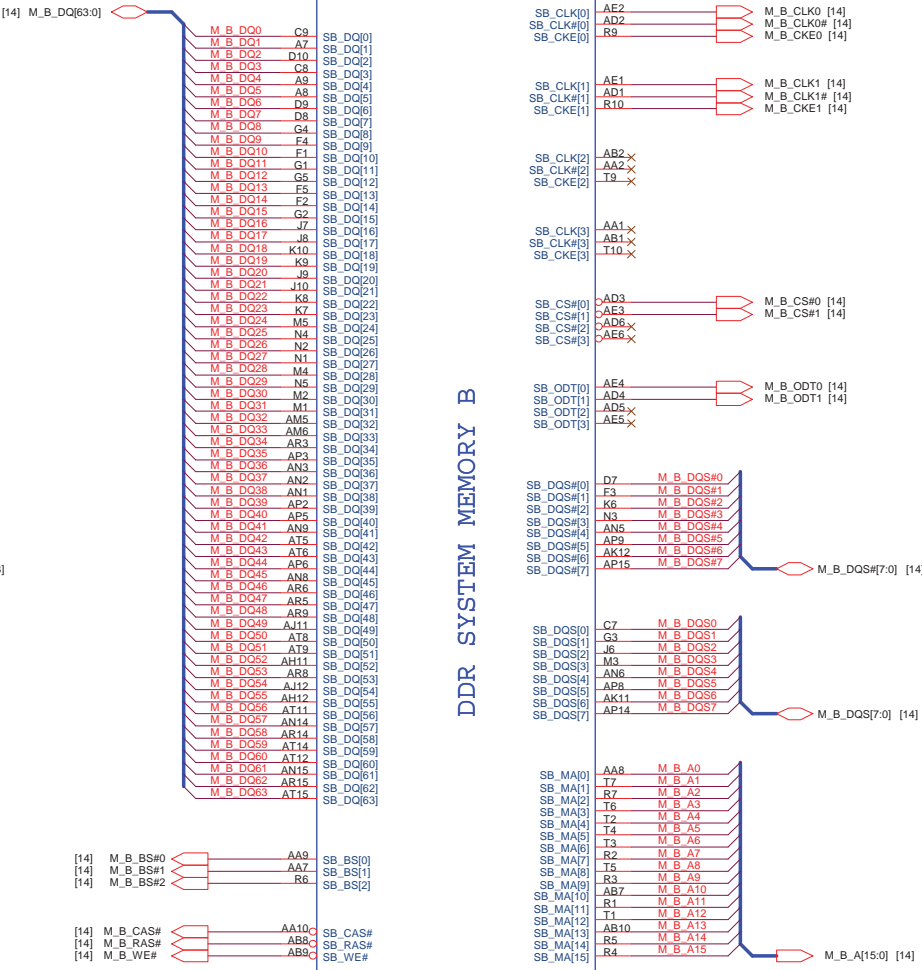
DDR SYSTEM MEMORY A



U16D

Ivy Bridge_rPGA_2DPC_Rev0p61

DDR SYSTEM MEMORY B



IVY Processor (POWER)

CPU Core Power

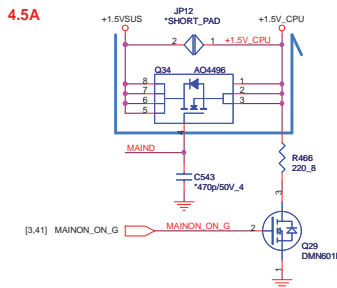
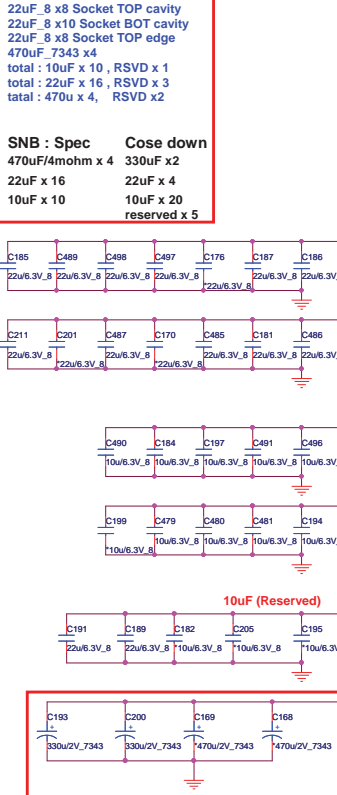
IVY 45W:TDC 52A

IVY SPEC

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4
total : 10uF x 10, RSVD x 1
total : 22uF x 16, RSVD x 3
total : 470u x 4, RSVD x 2

SNB : Spec Cose down
470uF/4mohm x 4 330uF x 2
22uF x 16 22uF x 4
10uF x 10 10uF x 2
reserved x 5

POWER



CPU VTT
IVY 45W:8.5A
SNB : Spec
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)

Cose down
330uF x 1
22uF x 2
10uF x 10
reserved x 4

CPU VGT
IVY 45W:TDC 38A
Spec
470uF/4mohm x 2
22uF x 12

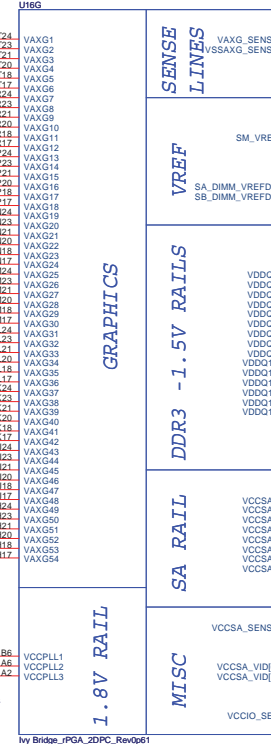
Cose down
330uF x 1
22uF x 4
10uF x 10

IVY SPEC
22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

IVY Bridge Processor (GRAPHIC POWER)

POWER

0929 change value by CRB



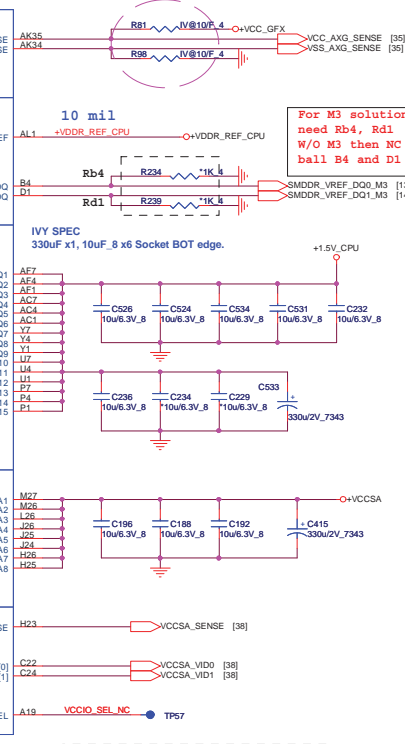
SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC



CPU VCCPL

IVY 45W:1.5A

Spec

330uF/7mohm x 1

10uF x 1

10uF x 2

1uF x 2

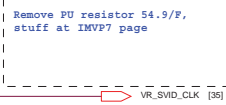
IVY SPEC

330uF x 1, 10uF_8 x 1, 1uF_4 x 2

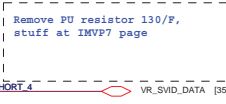
Socket BOT edge.

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK



SVID DATA



SVID ALERT



IVY SPEC
330uF x 1, 10uF_8 x 1 Socket BOT edge,
10uF_8 x 2 Socket BOT cavity.

CPU SA

IVY 45W: 6A

Spec

330uF/7mohm x 1

10uF x 3

Real

10uF x 8

CPU MCH

IVY 45W: 5A

Spec

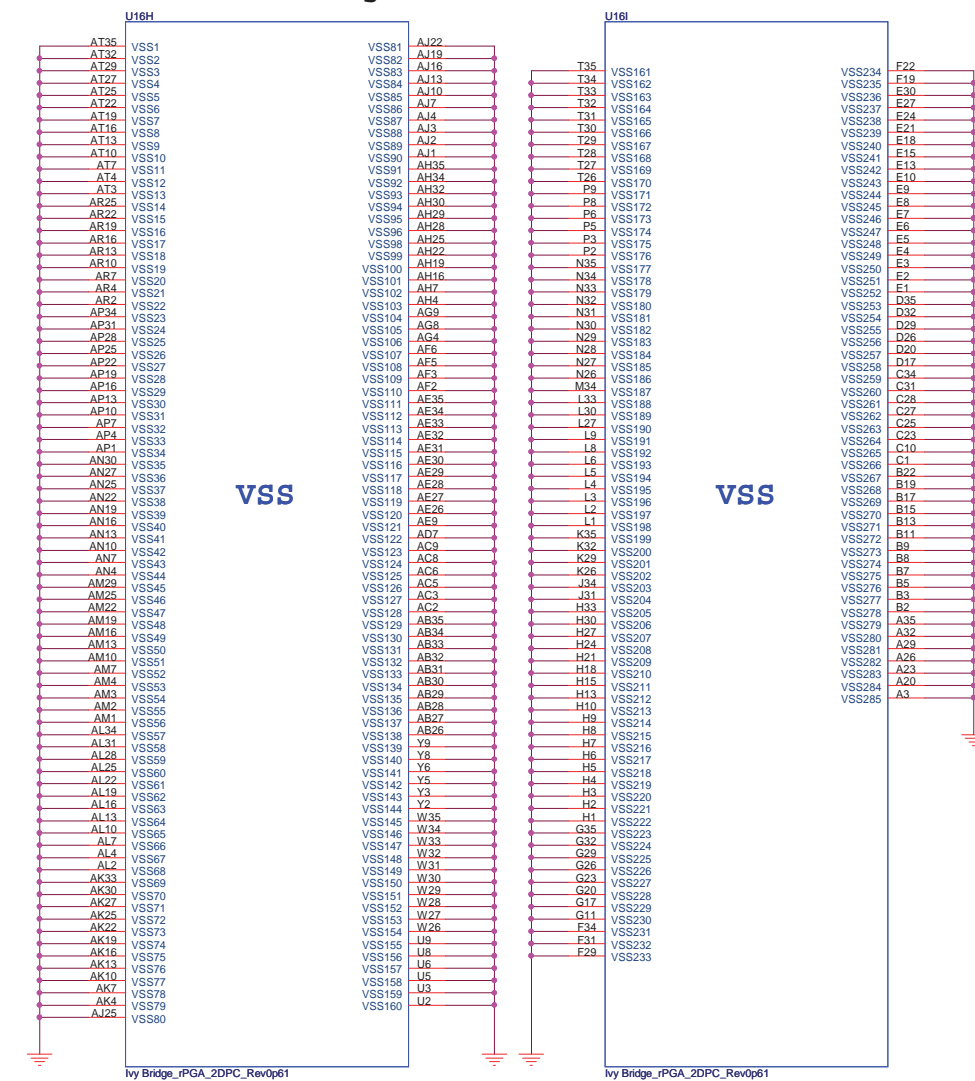
330uF/6mohm x 1

10uF x 6

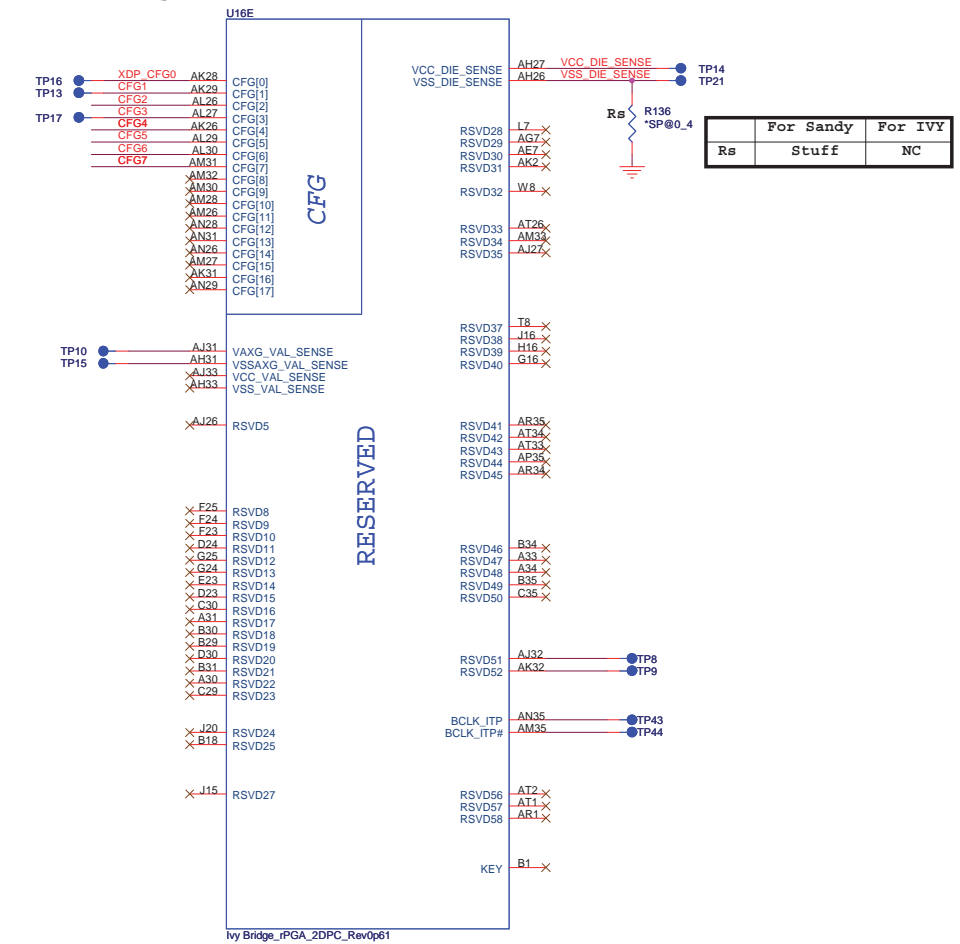
Real

10uF x 8

IVY Bridge Processor (GND)



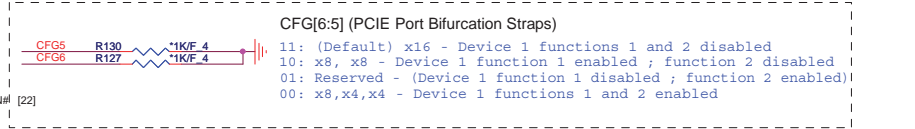
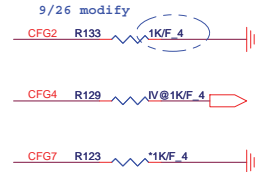
IVY Bridge Processor (RESERVED, CFG)



Processor Strapping

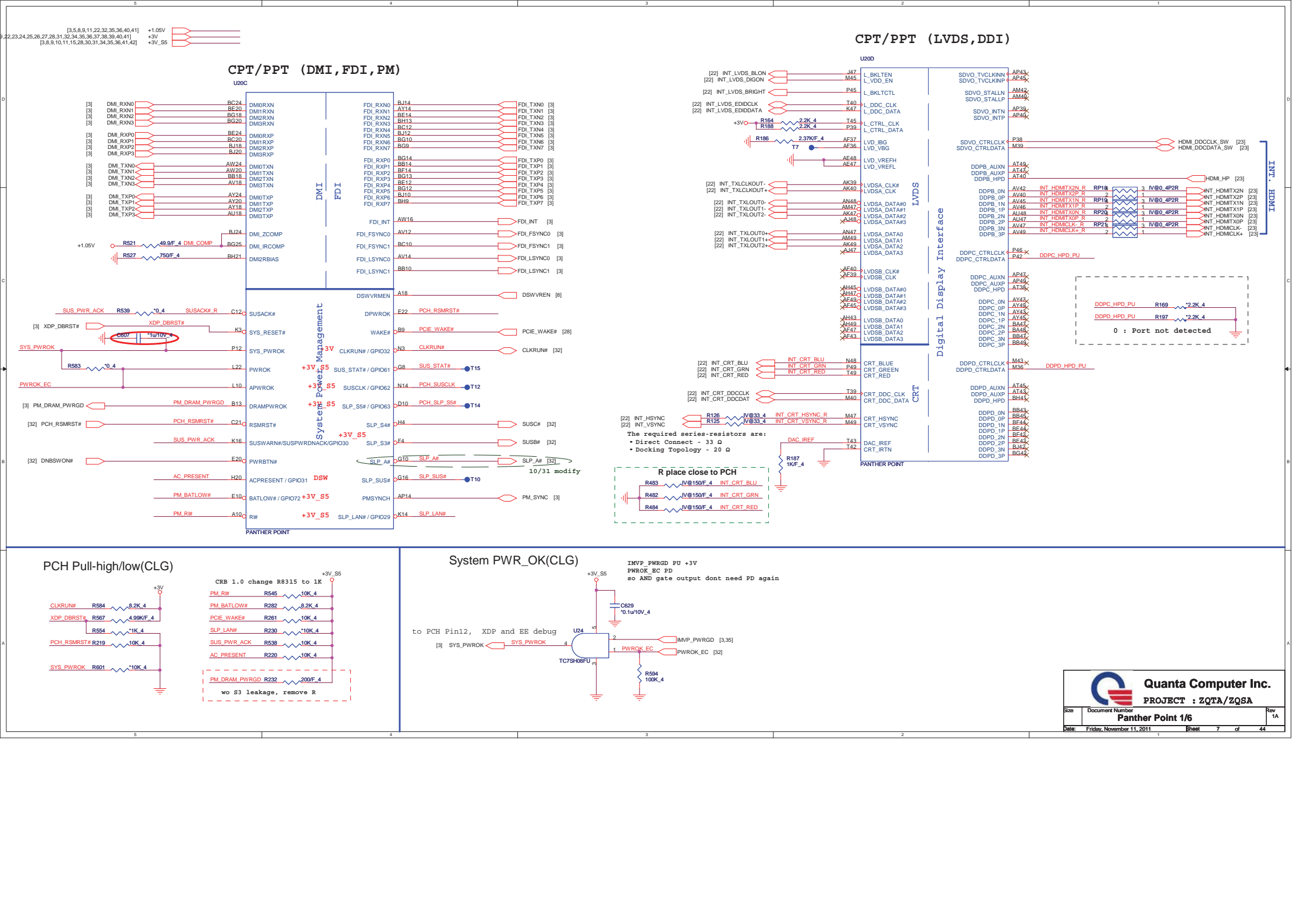
The CFG signals have a default value of '1' if not terminated on the board.

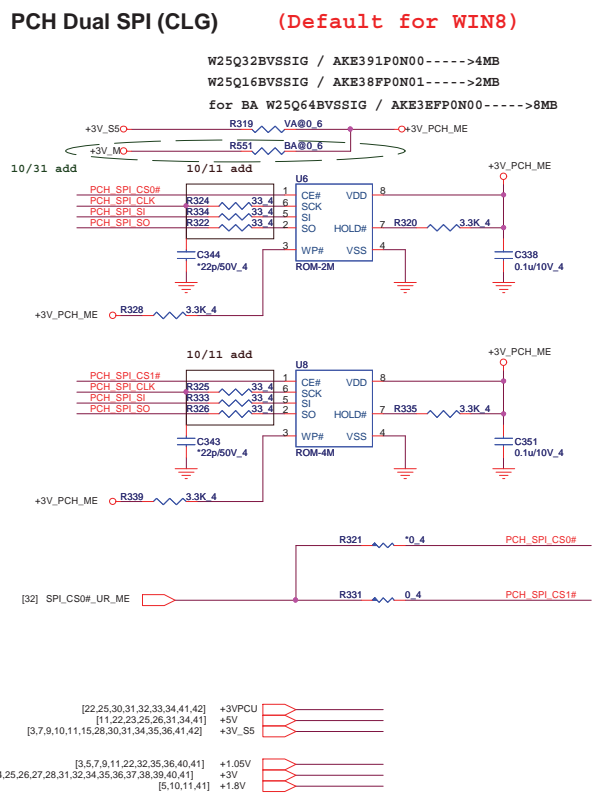
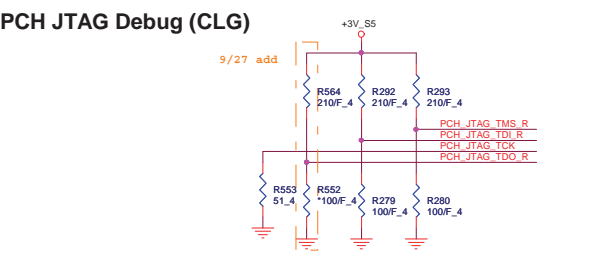
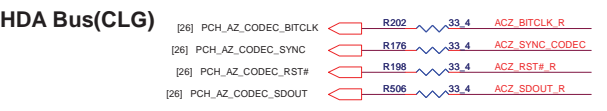
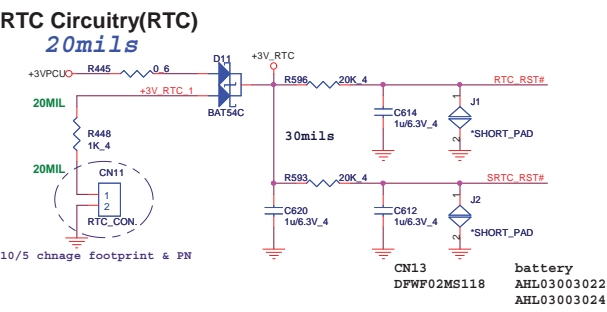
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



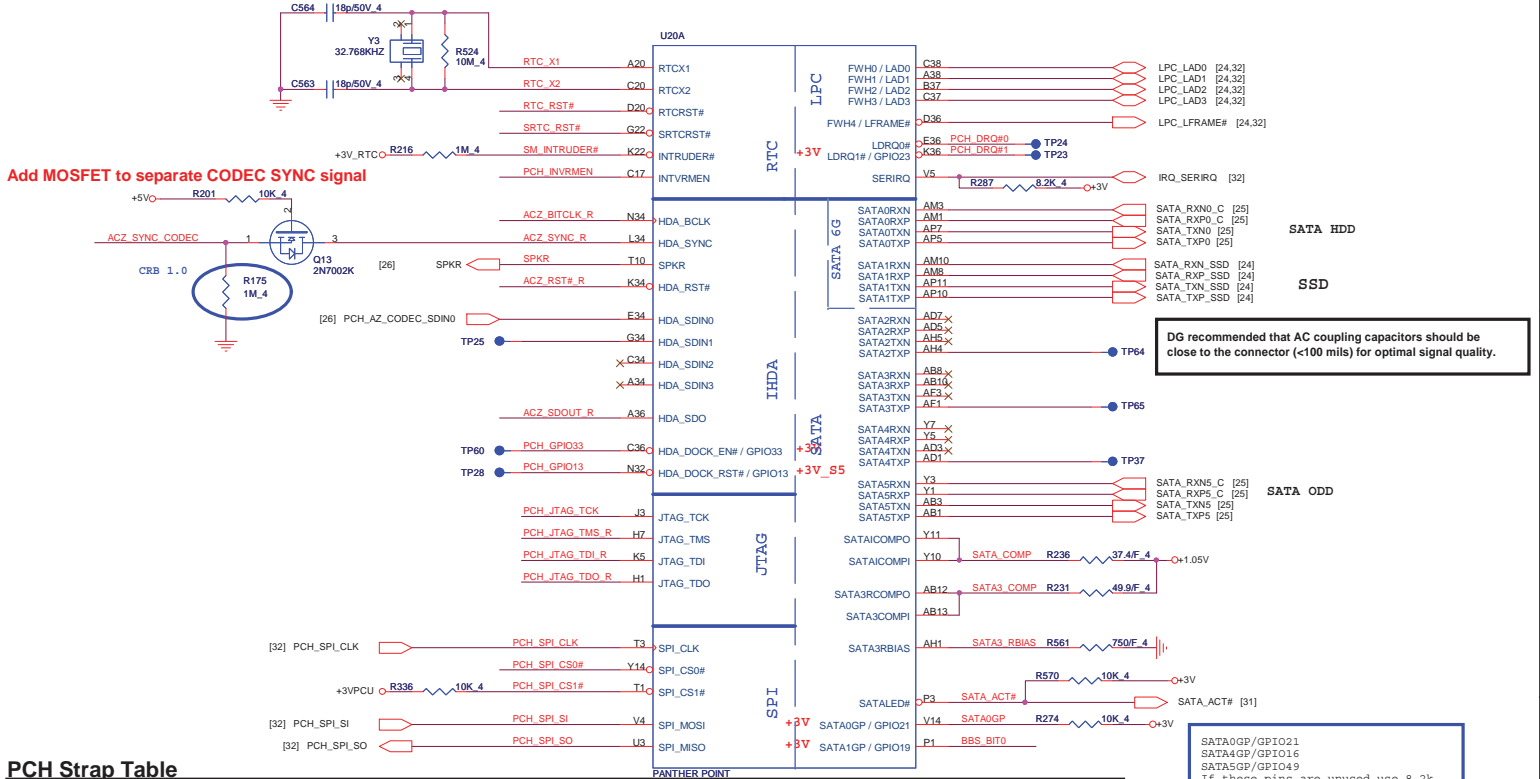
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	IVY Bridge 4/4	1A
Date:	Friday, November 11, 2011	Sheet 6 of 44





PCH2 (CLG) CPT/PPT (HDA, JTAG, SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V_ R301 1K 4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R171 1K 4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R526 330K 4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden	32 ME_WR R505 SHORT 4 ACZ_SDOOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc	R548 2.2K 4 0.1.8V R546 1K 4 H_SNB_IVB# [3] DF_TVS [10] 0930
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	R277 1K 4 PLL_ODVR_EN [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R177 1K 4 ACZ_SYNC_R
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable	+3V_S5 R563 1K 4 PCH_GPIO15 [10]
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable	+3V_RTC R530 330K 4 DSWVREN [7] R528 330K 4
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R308 1K 4 INV_ALE [9]

U20

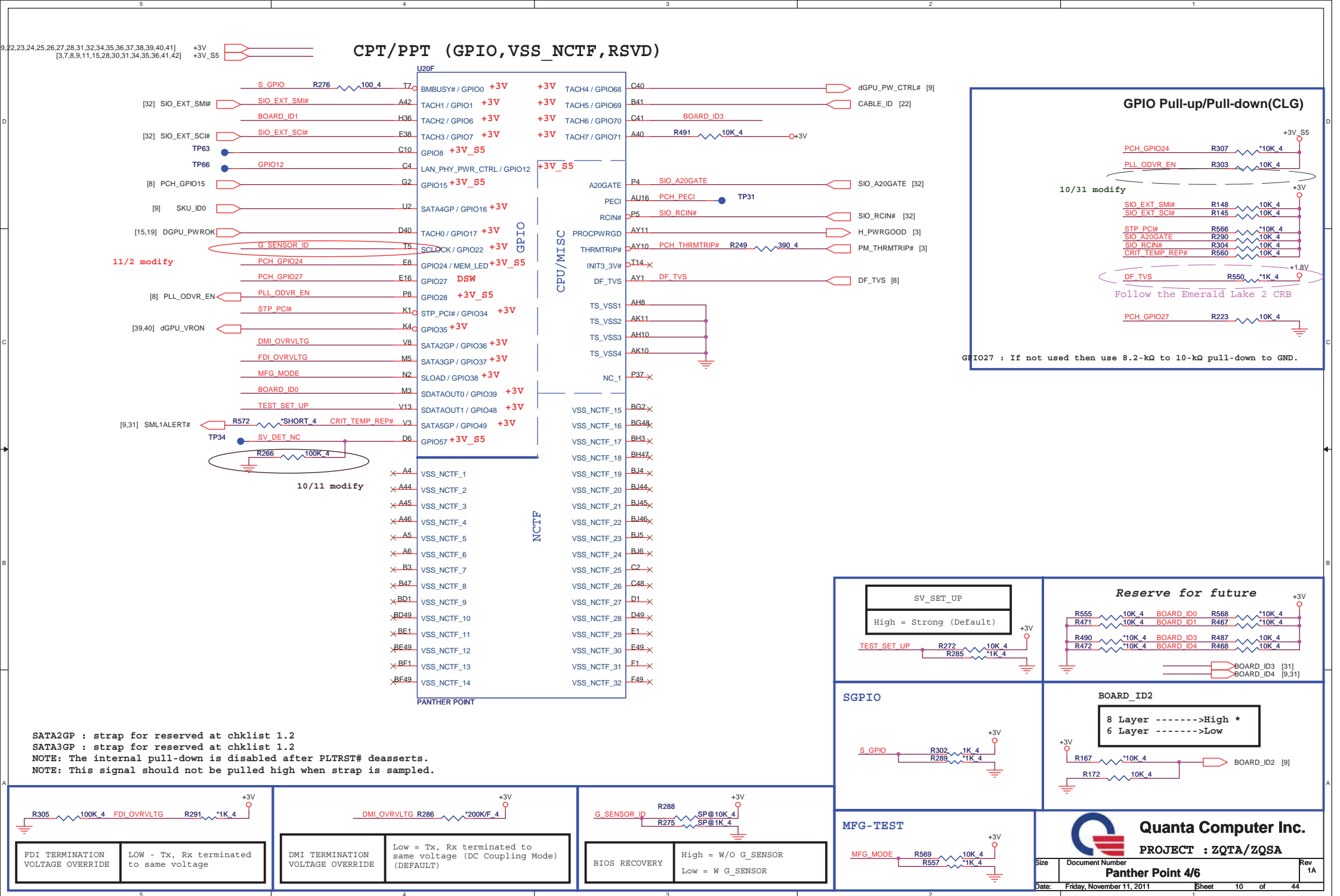


The schematic diagram shows two components, S5 and S0, connected to a +3V supply. S5 is a 3-bit bus component with inputs SMB_PCH_DAT[3:1] and output CLK_SDATA[13:14,24:25]. S0 is a 1-bit component with input CLK_SDATA[13:14,24:25] and output CLK_SDATA[13:14,24:25]. The components are connected via a 4.7K pull-up resistor R8003 to a +3V supply.

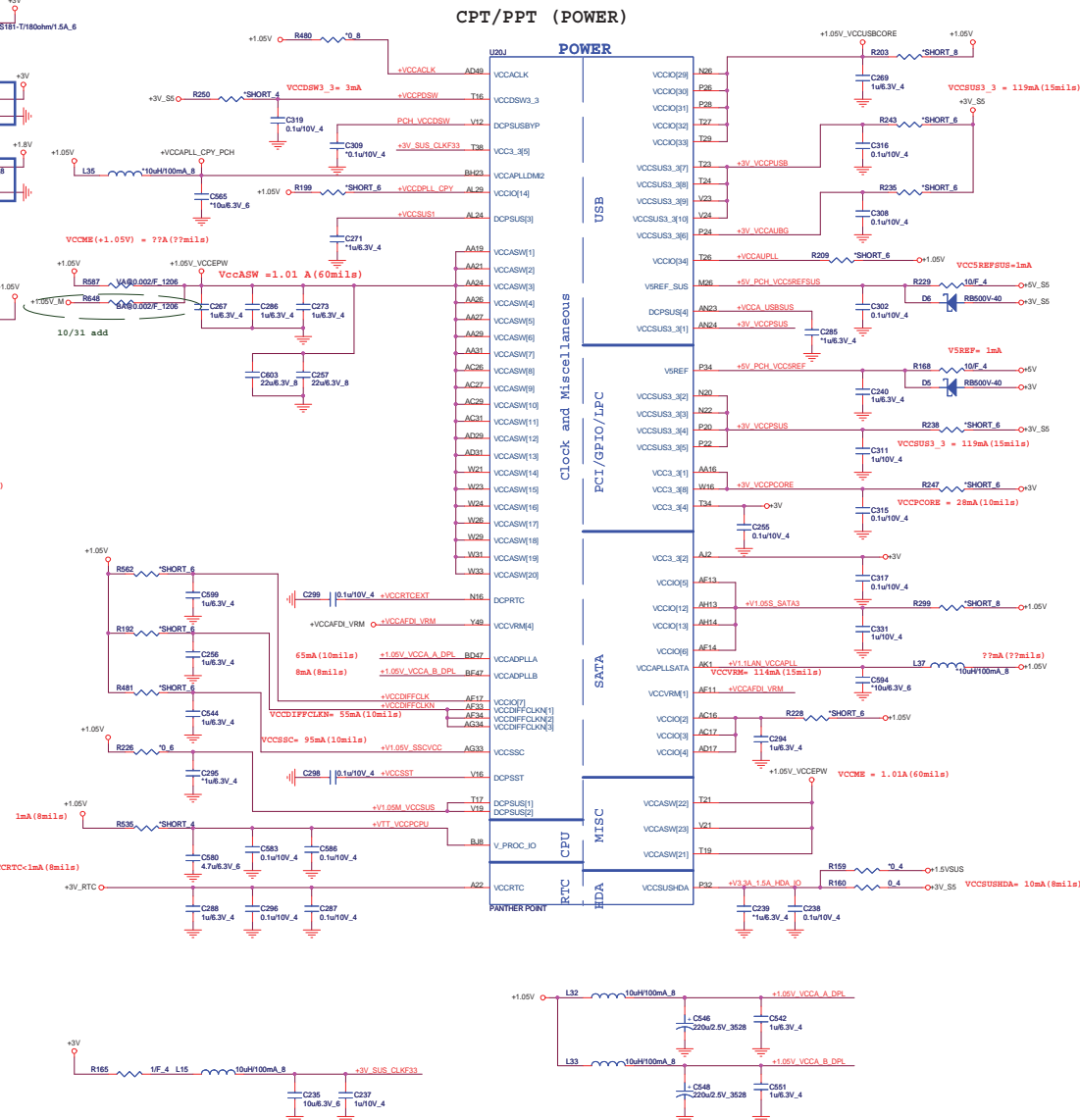
	GPIO_PW_CTLS (GPIO4) (CTL = GPIO_VBUS)	SEQ_ID1 (GPIO4)	SEQ_ID0 (GPIO16)	UMA_R/W Signal	Setup
UMA Only	1	0	0	UMA	Hidden
GPU Only	0	0	1	GPU	Hidden
Swichable (Flex)				UMA/GPU	GPU boot
Optimise (Busless)	0	1	1	UMA	UMA/SG

GPIO_PW_CTLS
0 = GPU power is control by R/W (pure Discrete SEQ)
1 = GPU power is control by PCH GPIO (Discrete, SG or Optimise)
--->[Default]

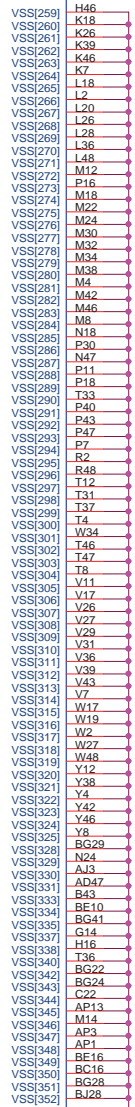
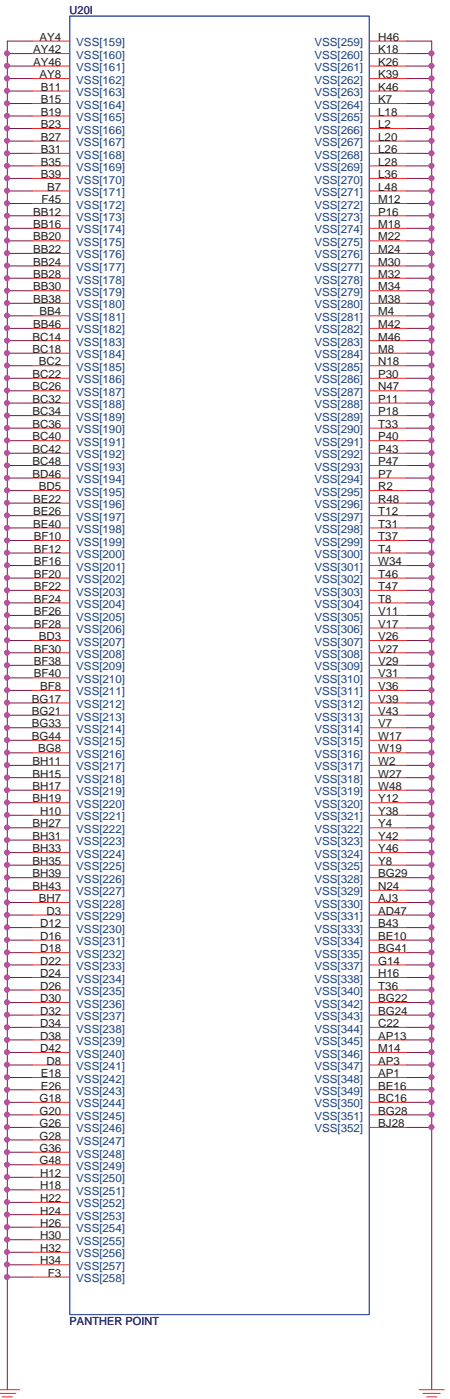
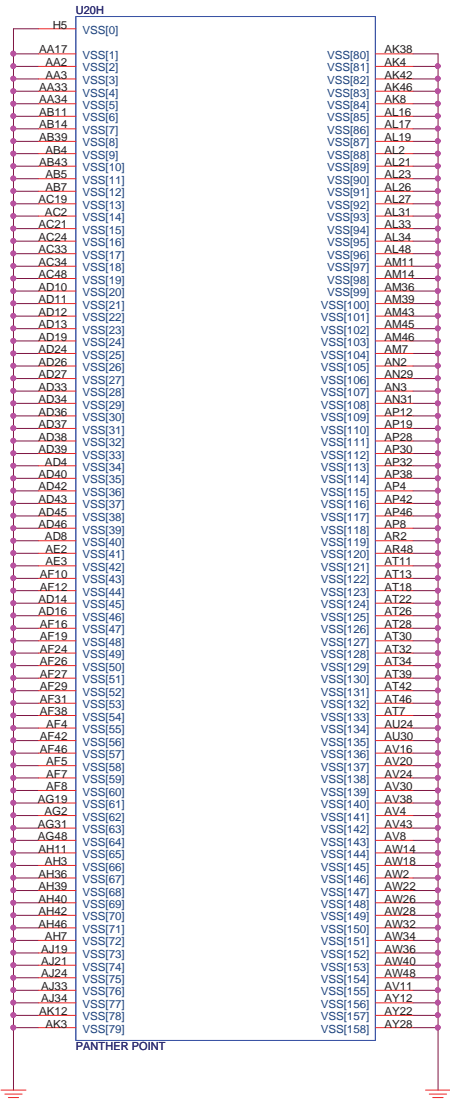
Schematic diagram of the DRAM controller interface. It shows a 2N7000K MOSFET with its gate connected to the [32] 2ND_MBDATA signal and its drain connected to the SMB_MF1 signal through a 2.9K₄ resistor. The source of the MOSFET is connected to the +3V_S5 supply. The MOSFET's gate is also connected to a 1K₄ resistor, which is in turn connected to the DRAMRST_CNTRL_PCH signal. The MOSFET's drain is also connected to a 10K₄ resistor, which is in turn connected to the DRAMRST_CNTRL_PCH signal. The MOSFET's source is also connected to a 10K₄ resistor, which is in turn connected to the DRAMRST_CNTRL_PCH signal. The MOSFET's source is also connected to a 10K₄ resistor, which is in turn connected to the DRAMRST_CNTRL_PCH signal.

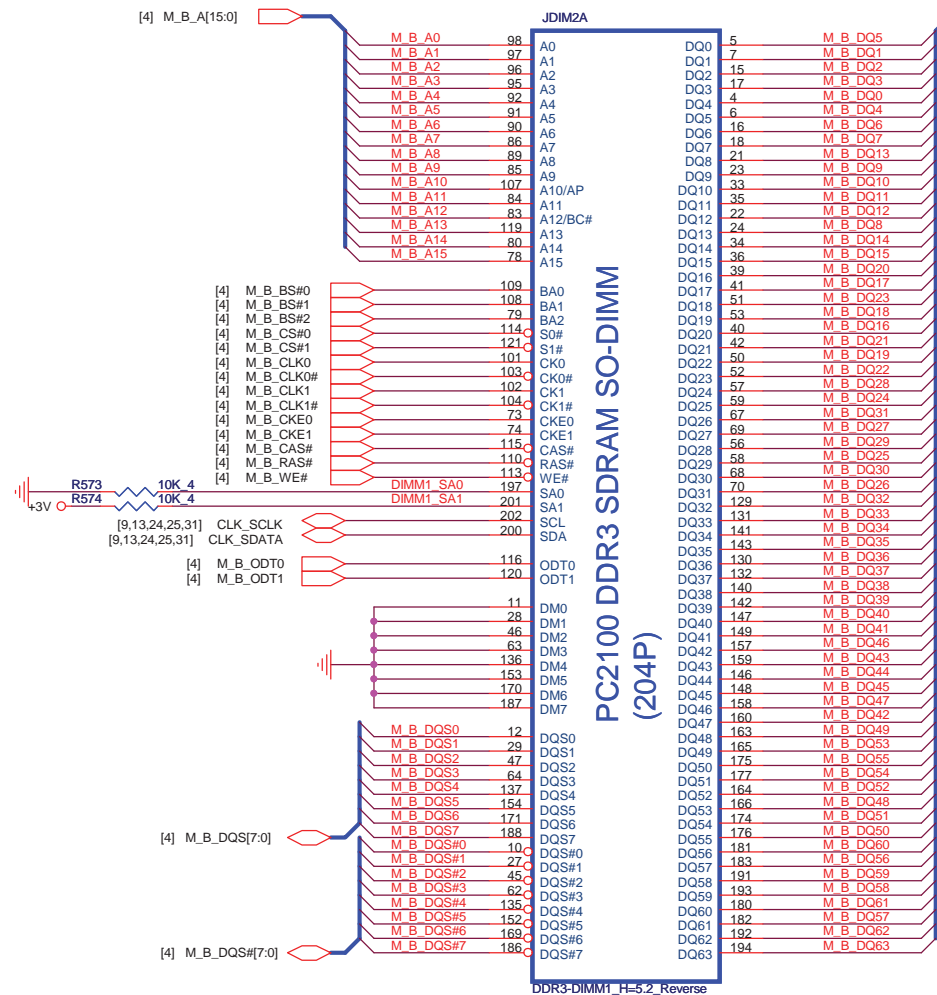


CPT/PPT (POWER)



IBEX PEAK-M (GND)





M_B_DQ[63:0] [4]

M3 solution

[5] SMDDR_VREF_DQ1_M3

R270 *M3@0 6

+SMDDR_VREF_DIMM

+SMDDR_VREF_DQ1

DDR3-DIMM1_H=5.2_Reverse

2.48A

3V

R529 *10K 4

PM_EXTTS#1

77

122

125

198

30

DDR3-DIMM1_H=5.2_Reverse

NC1

NC2

NCTEST

EVENT#

RESET#

VREF_DQ

VREF_CA

VSS1

VSS2

VSS3

VSS4

VSS5

VSS6

VSS7

VSS8

VSS9

VSS10

VSS11

VSS12

VSS13

VSS14

VSS15

VSS16

VSS17

VSS18

VSS19

VSS20

VSS21

VSS22

VSS23

VSS24

VSS25

VSS26

VSS27

VSS28

VSS29

VSS30

VSS31

VSS32

VSS33

VSS34

VSS35

VSS36

VSS37

VSS38

VSS39

VSS40

VSS41

VSS42

VSS43

VSS44

VSS45

VSS46

VSS47

VSS48

VSS49

VSS50

VSS51

VSS52

VTT1

VTT2

GND

GND

+0.75V_DDR_VTT

203

204

205

206

DDR3-DIMM1_H=5.2_Reverse

PC2100 DDR3 SDRAM SO-DIMM (204P)

2.48A

3V

R529 *10K 4

PM_EXTTS#1

77

122

125

198

30

DDR3-DIMM1_H=5.2_Reverse

NC1

NC2

NCTEST

EVENT#

RESET#

VREF_DQ

VREF_CA

VSS1

VSS2

VSS3

VSS4

VSS5

VSS6

VSS7

VSS8

VSS9

VSS10

VSS11

VSS12

VSS13

VSS14

VSS15

VSS16

VSS17

VSS18

VSS19

VSS20

VSS21

VSS22

VSS23

VSS24

VSS25

VSS26

VSS27

VSS28

VSS29

VSS30

VSS31

VSS32

VSS33

VSS34

VSS35

VSS36

VSS37

VSS38

VSS39

VSS40

VSS41

VSS42

VSS43

VSS44

VSS45

VSS46

VSS47

VSS48

VSS49

VSS50

VSS51

VSS52

VTT1

VTT2

GND

GND

+0.75V_DDR_VTT

203

204

205

206

DDR3-DIMM1_H=5.2_Reverse

PC2100 DDR3 SDRAM SO-DIMM (204P)

2.48A

3V

R529 *10K 4

PM_EXTTS#1

77

122

125

198

30

DDR3-DIMM1_H=5.2_Reverse

NC1

NC2

NCTEST

EVENT#

RESET#

VREF_DQ

VREF_CA

VSS1

VSS2

VSS3

VSS4

VSS5

VSS6

VSS7

VSS8

VSS9

VSS10

VSS11

VSS12

VSS13

VSS14

VSS15

VSS16

VSS17

VSS18

VSS19

VSS20

VSS21

VSS22

VSS23

VSS24

VSS25

VSS26

VSS27

VSS28

VSS29

VSS30

VSS31

VSS32

VSS33

VSS34

VSS35

VSS36

VSS37

VSS38

VSS39

VSS40

VSS41

VSS42

VSS43

VSS44

VSS45

VSS46

VSS47

VSS48

VSS49

VSS50

VSS51

VSS52

VTT1

VTT2

GND

GND

+0.75V_DDR_VTT

203

204

205

206

DDR3-DIMM1_H=5.2_Reverse

PC2100 DDR3 SDRAM SO-DIMM (204P)

2.48A

3V

R529 *10K 4

PM_EXTTS#1

77

122

125

198

30

DDR3-DIMM1_H=5.2_Reverse

NC1

NC2

NCTEST

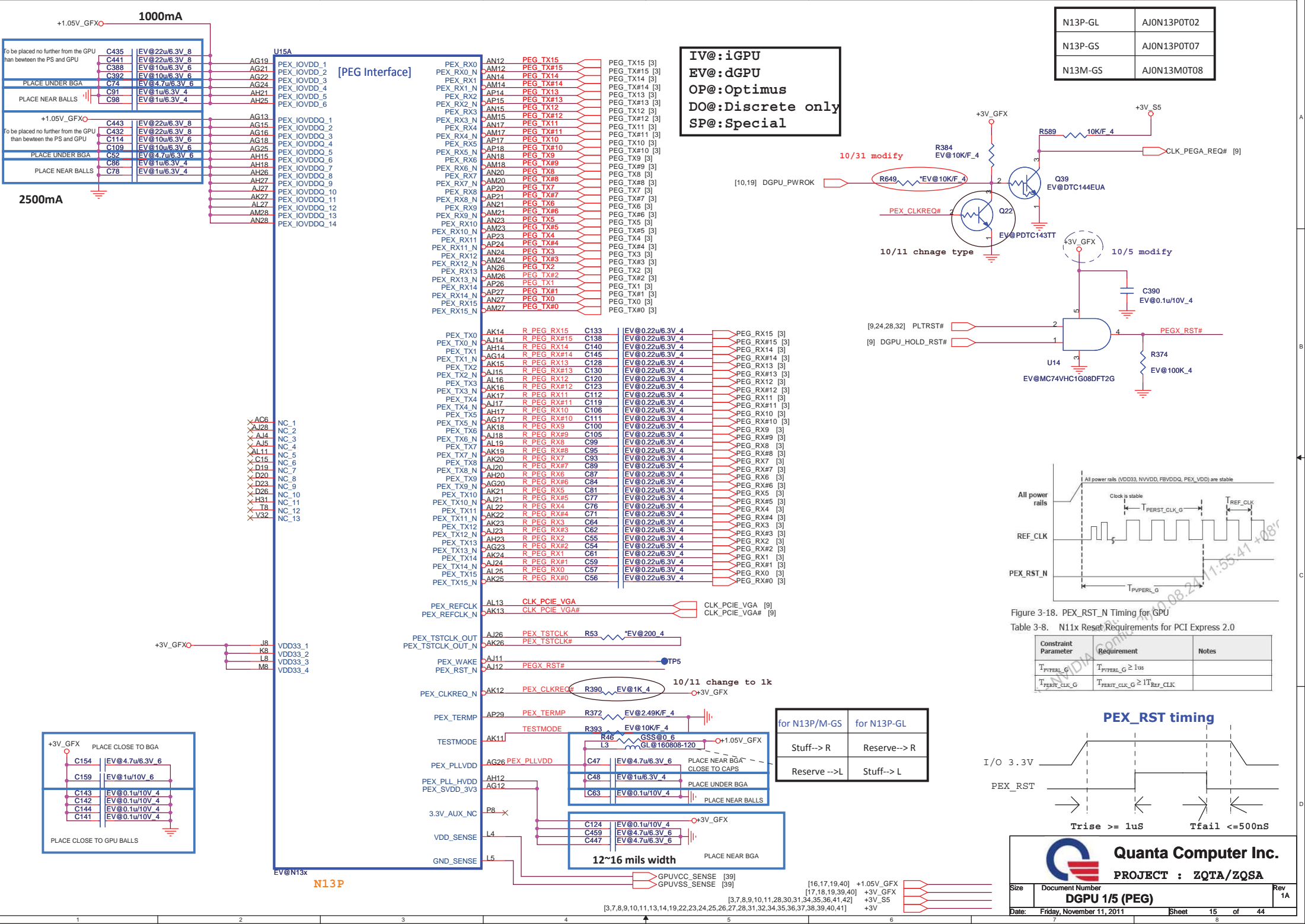
EVENT#

RESET#

VREF_DQ

VREF_CA

VSS1</



N13P-GL	AJON13P0T02
N13P-GS	AJON13P0T07
N13M-GS	AJON13M0T08

IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

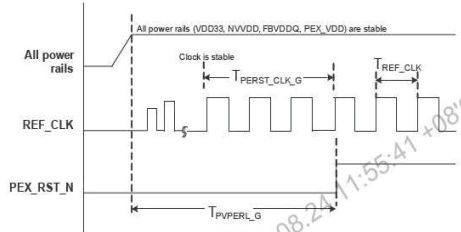
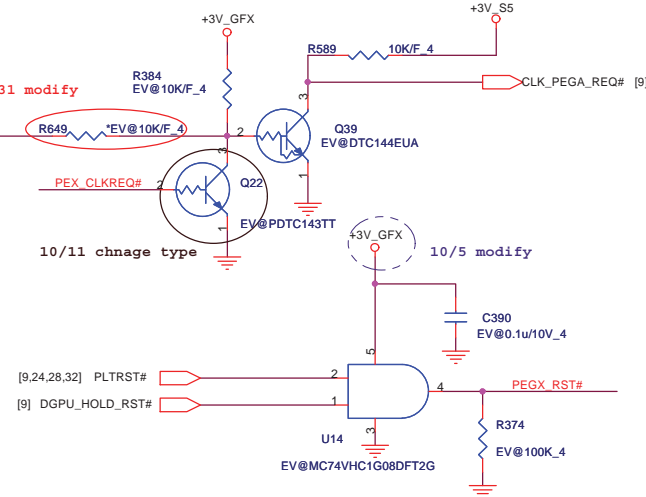
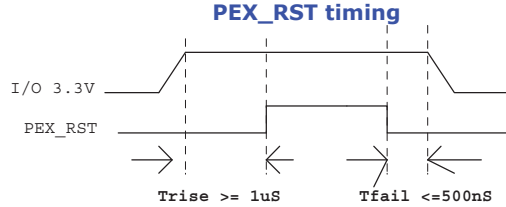
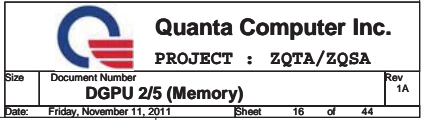


Figure 3-18. PEX_RST_N Timing for GPU
Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T _{FWPERL_G}	T _{FWPERL_G} ≥ 1μs	
T _{PERST_CLK_G}	T _{PERST_CLK_G} ≥ 1T _{REF_CLK}	

	for N13P/M-GS	for N13P-GL
Stuff--> R	Reserve--> R	
Reserve -->L	Stuff--> L	





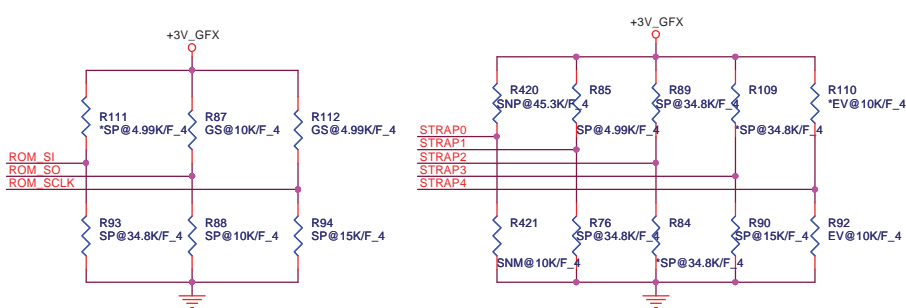
[15,17,19,39,40] +3V_GFX

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N13P-GL	AJ0N13P0T02
N13P-GS	AJ001070T00
N13M-GS	AJ001170T00

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1110
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0010
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	0011



N13P-GS/-GL Strapping table

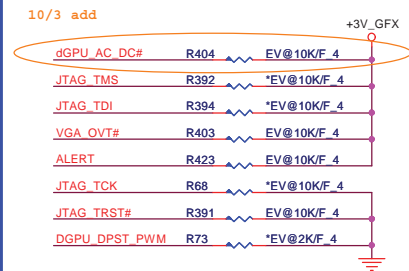
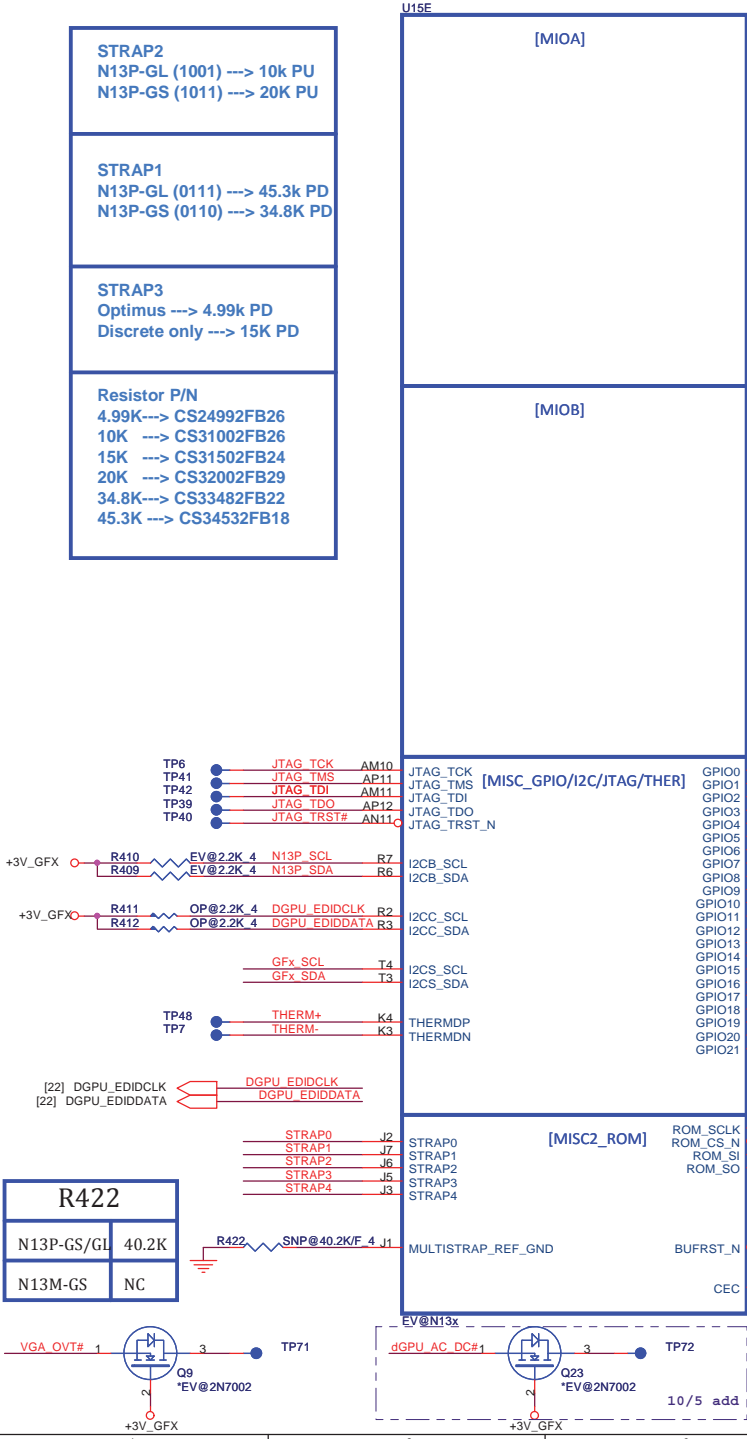
ROM_SI	1G Hynix 64Mx16 -->15K PD 1G Micron 64Mx16 -->20K PD 2G Hynix 128Mx16 -->35K PD (Default) 2G Micron 128Mx16 -->45K PD	ROM_SO N13P-GL --> 10K PD N13P-GS --> 10K PU	ROM_SCLK N13P-GL (0010) --> 15k PD N13P-GS (1000) --> 4.99K PU
--------	--	--	--

N13M-GS Strapping table

Pin Name	Strap Mapping	Value
ROM_SCLK	SMB_ALT_ADDR	0
ROM_SI	SUB_VENDOR	0
ROM_SO	VGA_DEVICE	0
STRAP[3..0]	RAM_CFG[3..0]	0010(Hynix 64Mx16) 0110(Hynix 128Mx16)
STRAP[4]	PCIE_MAX_SPEED	0

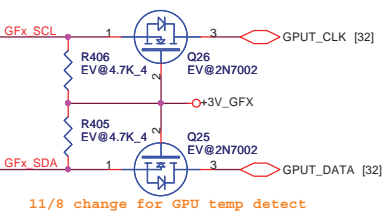
Remark :

0 -> 10K PD
1 -> 10K PU



10/3 modify

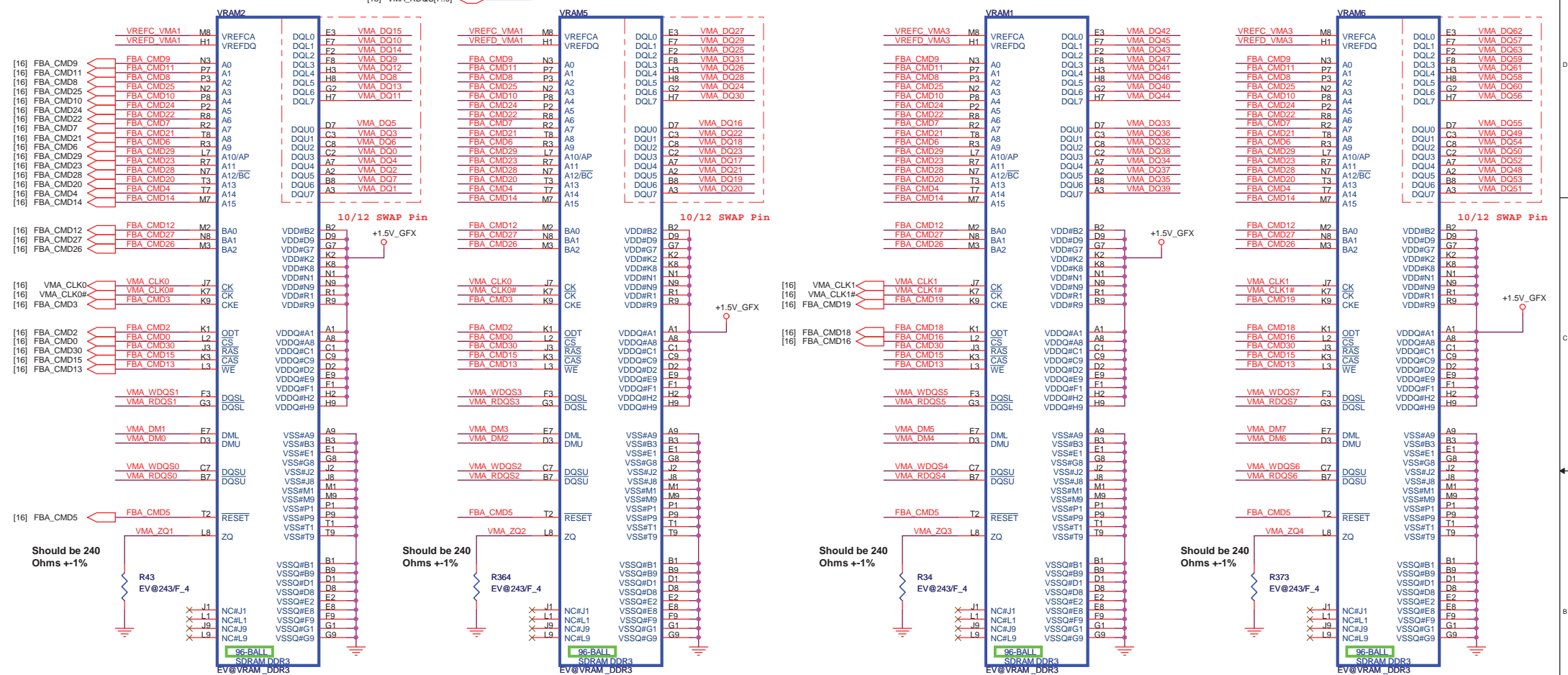
GFx SMBus Isolation



for N13P/M-GS	for N13P- GL
Reserve R108	Stuff R108



CHANNEL A: 256MB/512MB DDR3

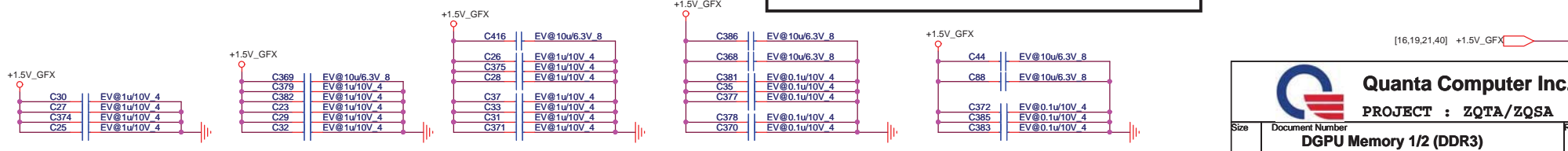


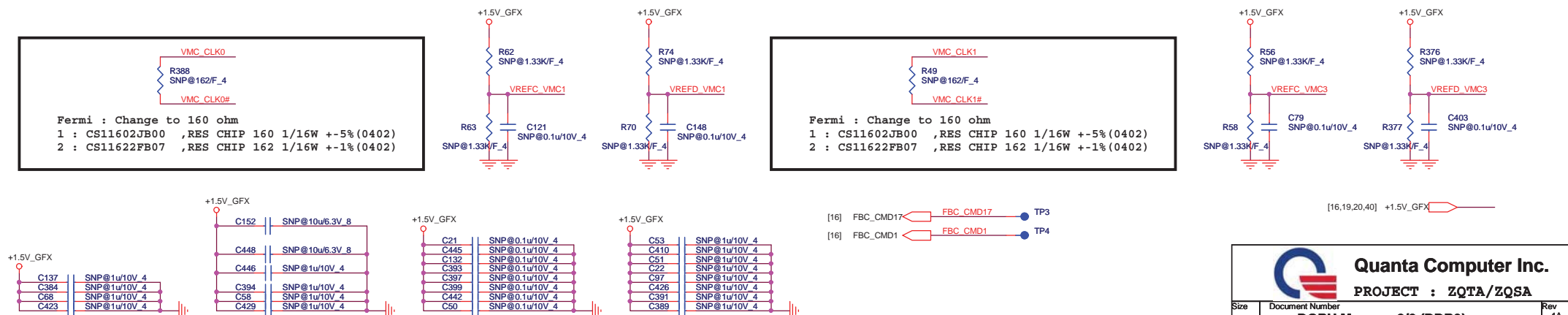
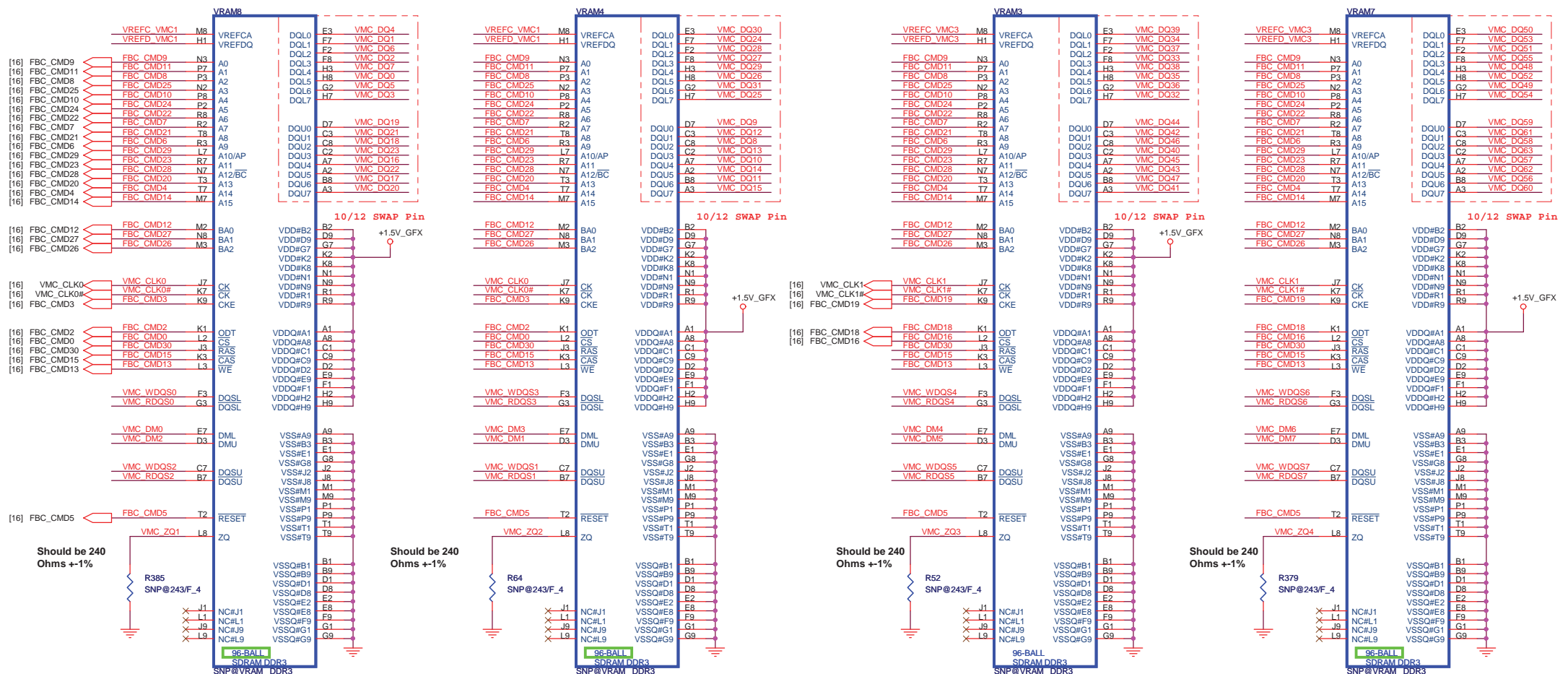
VMA_CLK0
R371 EV@162/F_4

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)

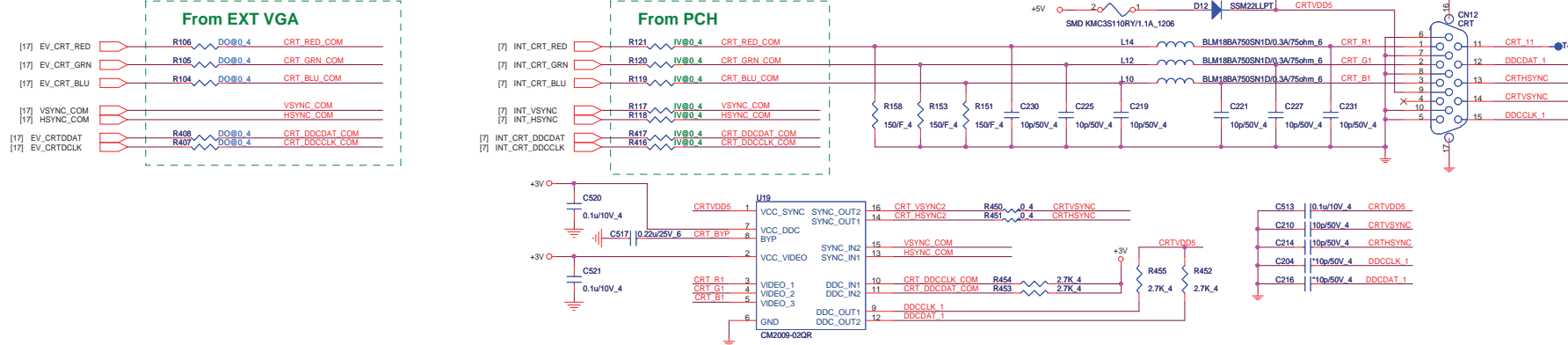
VMA_CLK1#
R41 EV@162/F_4

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)

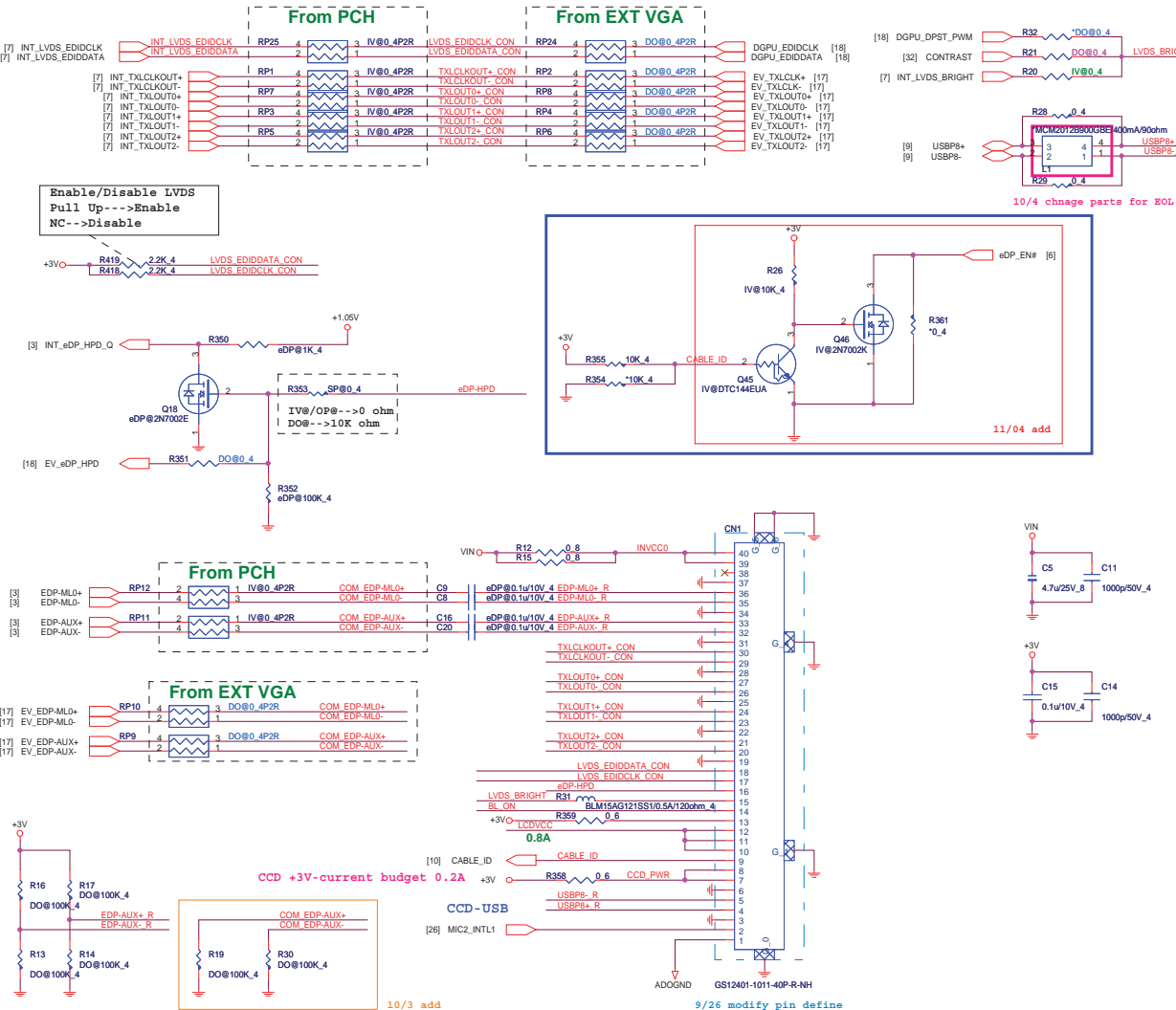




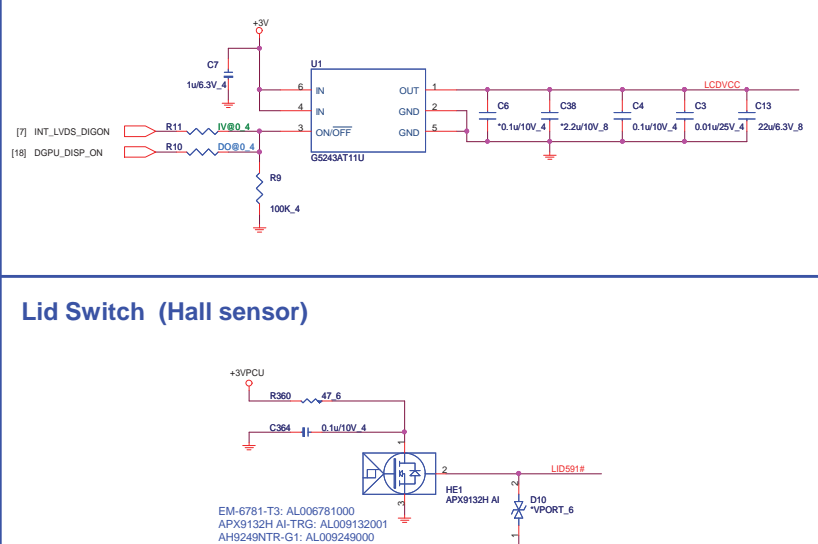
CRT



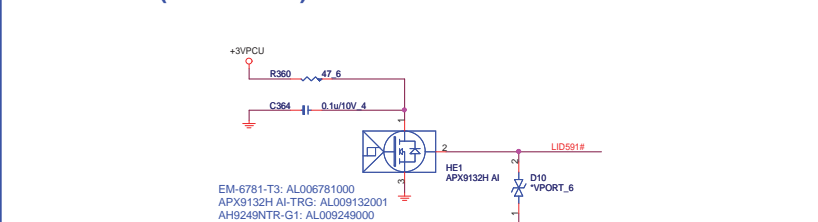
LVDS & eDP



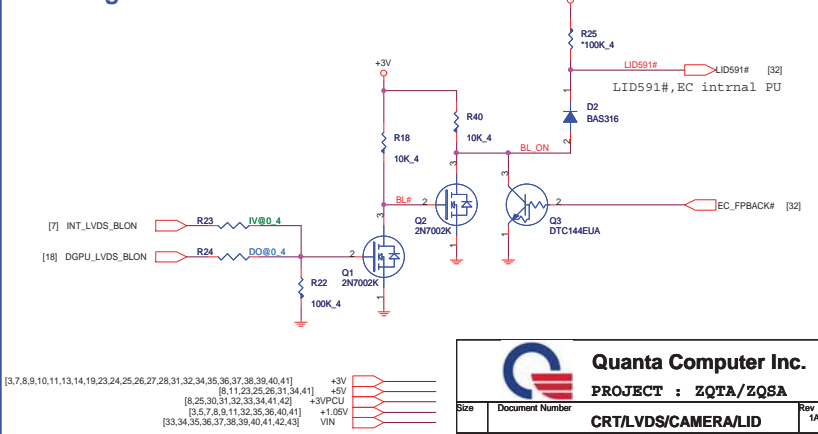
LCD Power



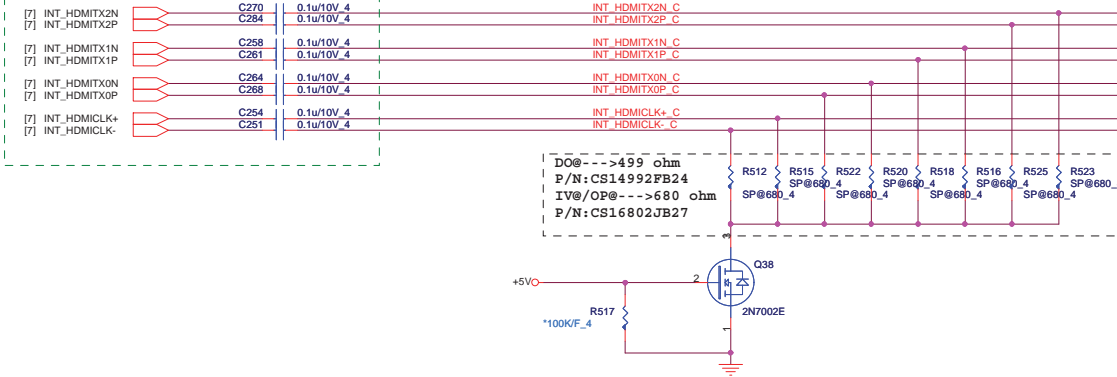
Lid Switch (Hall sensor)



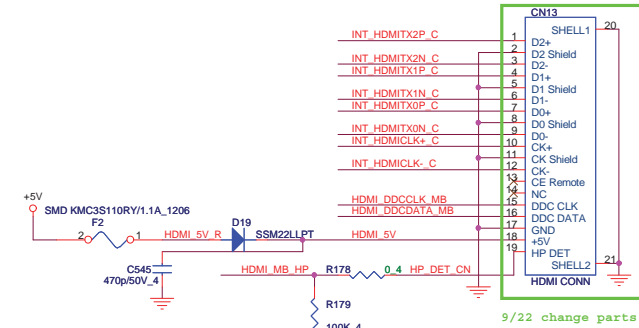
Backlight Control



From PCH



HDMI connector

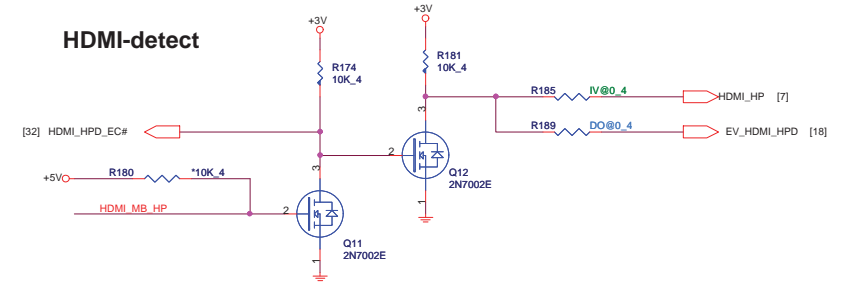


From EXT VGA



IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

HDMI-detect



I2C

UMA	R239 R245	CS22202JB18
DIS	R239 R245	CS24702JB38

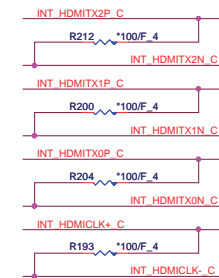
From EXT VGA



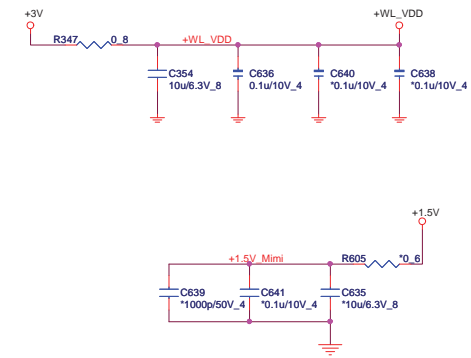
From PCH



EMI



+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



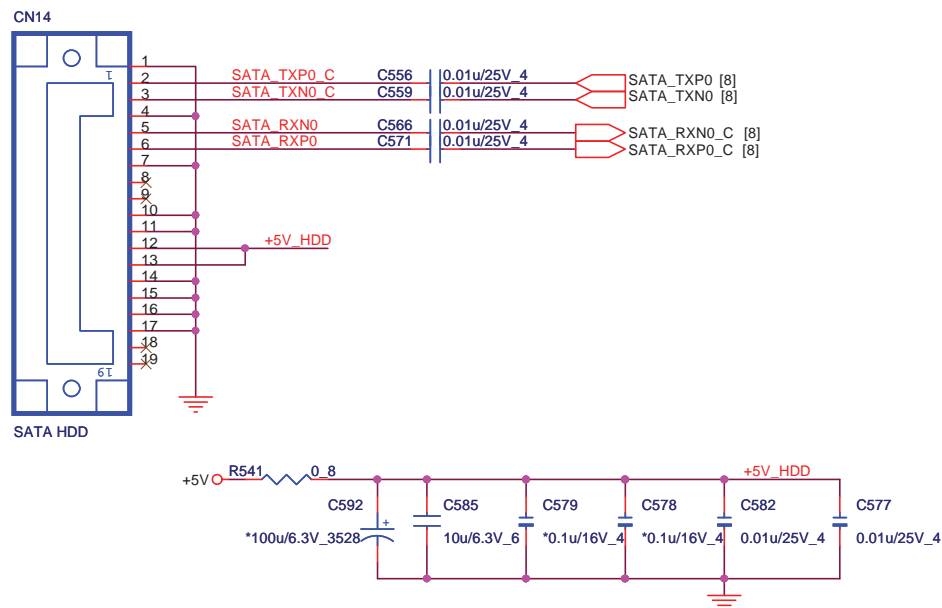
The diagram illustrates the pinout for the CN7 connector on the MINI-CARD1 module. The connector has 50 pins, with pins 1 through 50 labeled on the left and right sides. The pinout is as follows:

- Pin 1: Reserved
- Pin 2: Reserved
- Pin 3: Reserved
- Pin 4: Reserved
- Pin 5: Reserved
- Pin 6: Reserved
- Pin 7: Reserved
- Pin 8: Reserved
- Pin 9: Reserved
- Pin 10: Reserved
- Pin 11: REFCLK+
- Pin 12: REFCLK-
- Pin 13: GND
- Pin 14: CLREFQ#
- Pin 15: Reserved
- Pin 16: Reserved
- Pin 17: WAKE#
- Pin 18: GND
- Pin 19: GND
- Pin 20: GND
- Pin 21: UIM_C4
- Pin 22: UIM_C8
- Pin 23: PERn0
- Pin 24: PERp0
- Pin 25: GND
- Pin 26: SMB_CLK
- Pin 27: SMB_DATA
- Pin 28: PETp0
- Pin 29: GND
- Pin 30: GND
- Pin 31: GND
- Pin 32: GND
- Pin 33: GND
- Pin 34: GND
- Pin 35: GND
- Pin 36: GND
- Pin 37: GND
- Pin 38: GND
- Pin 39: GND
- Pin 40: GND
- Pin 41: +3.3Vaux
- Pin 42: LED_WPAN#
- Pin 43: LED_WLAN#
- Pin 44: LED_WWAN#
- Pin 45: GND
- Pin 46: GND
- Pin 47: GND
- Pin 48: GND
- Pin 49: GND
- Pin 50: GND

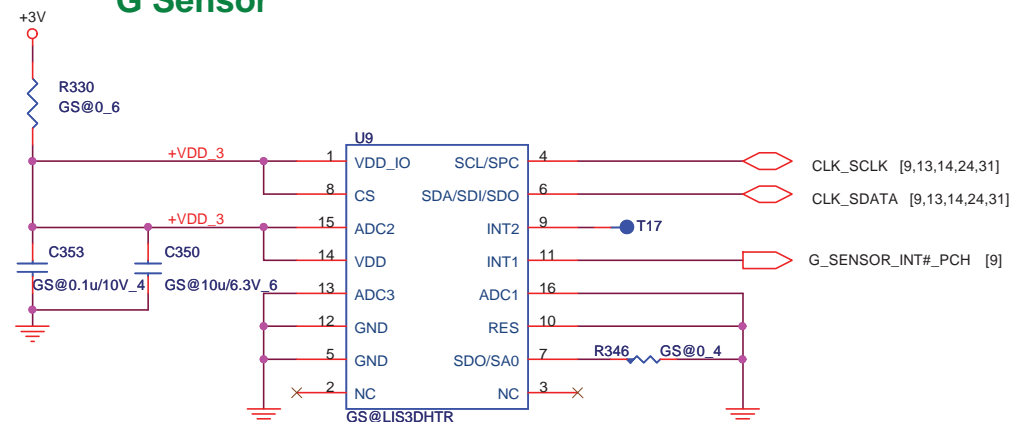
The diagram also shows the following components and connections:

- Capacitors: C616 (0.1u/10V_4), C615 (0.1u/10V_4), C647 (10u/10V_8).
- Resistor: R615 (0.8).
- Power supply: +3V_SATA.
- Connector: CN7.
- Module: MINI-CARD1.

MAIN SATA HDD(HDD)

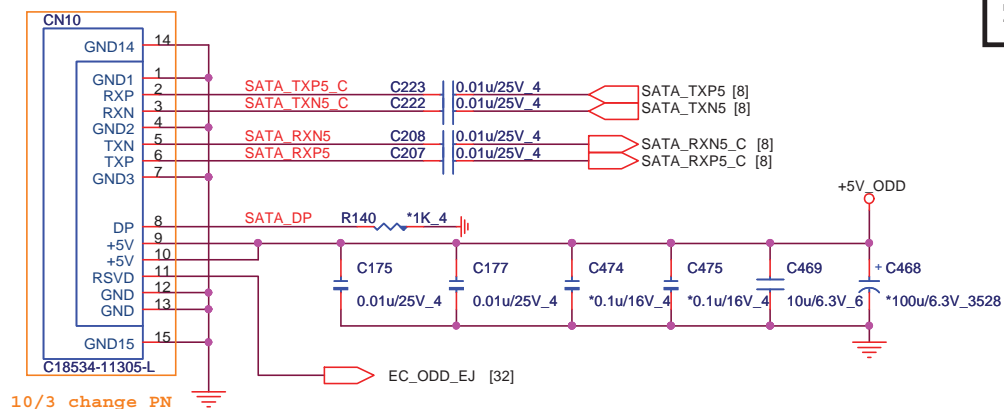


G Sensor



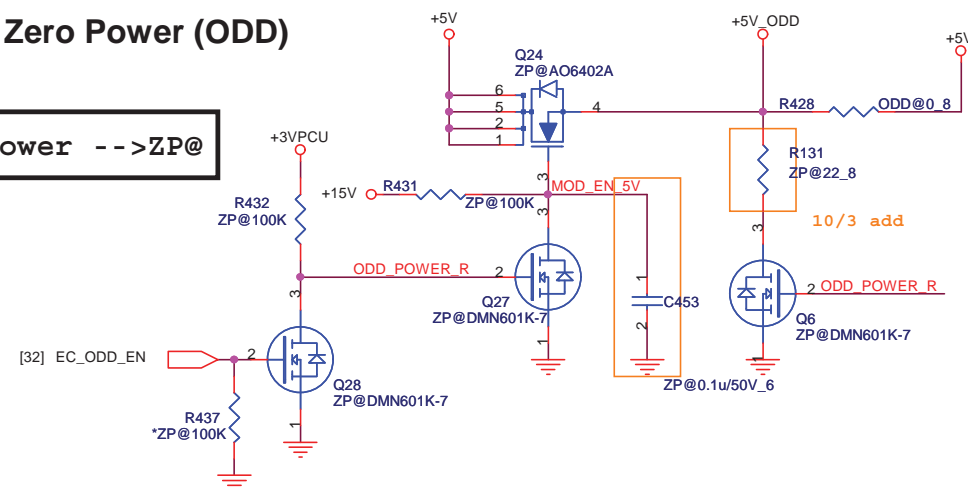
G-Sensor -->GS@

ODD (ODD)



Zero Power (ODD)

Zero Power --> ZP@



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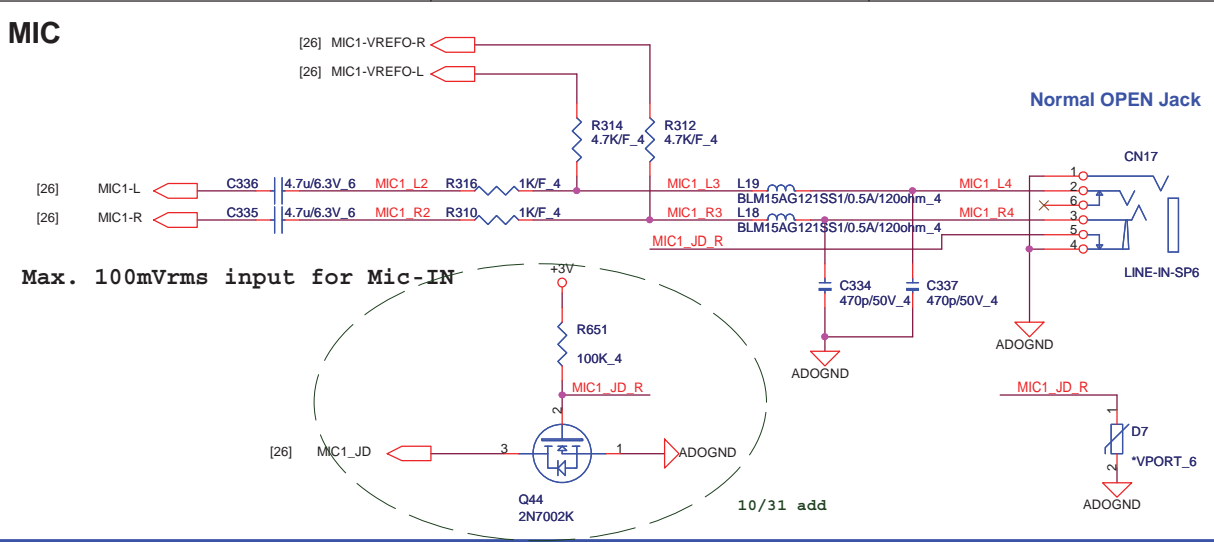
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	SATA-HDD/ODD/G Sensor	1A
Date:	Friday, November 11, 2011	Sheet 25 of 44

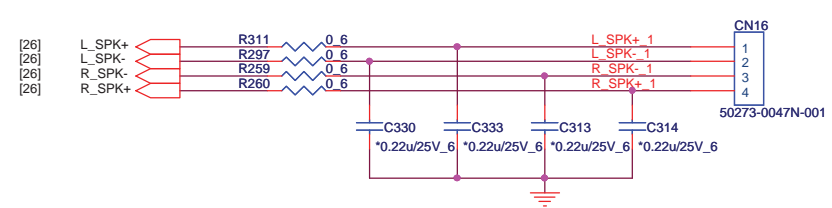
Date: Friday, November 11, 2011 Sheet 25 of 44

MIC

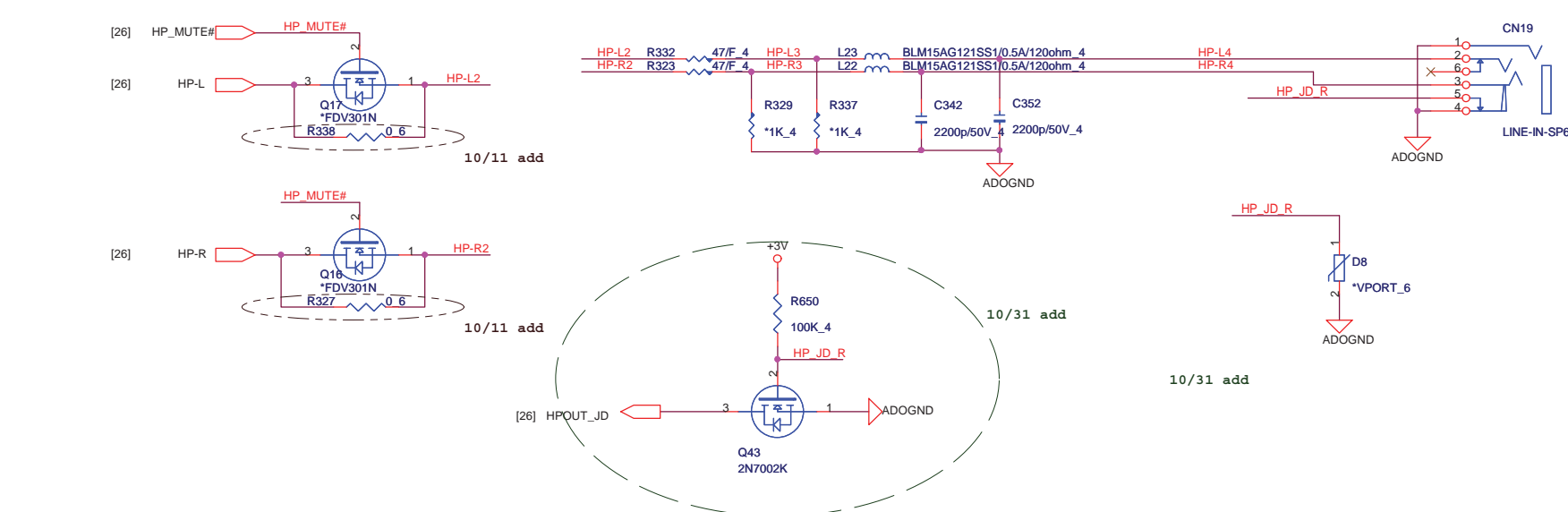
Max. 100mVrms input for Mic-IN



Internal Speaker



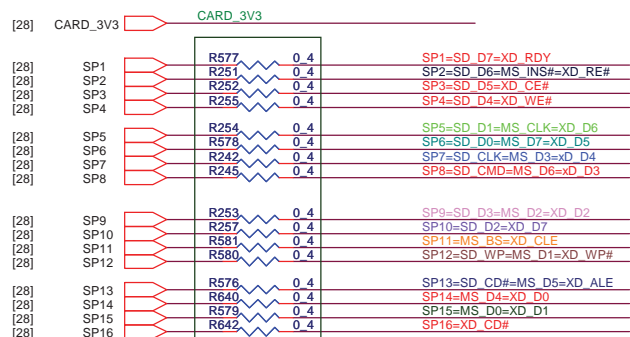
HP



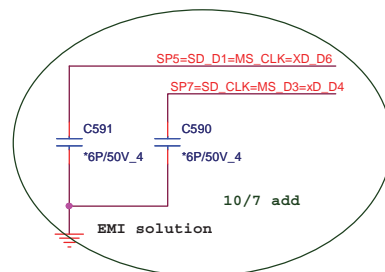
CARD READER CONNECTOR

Share Pin

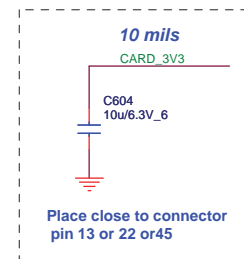
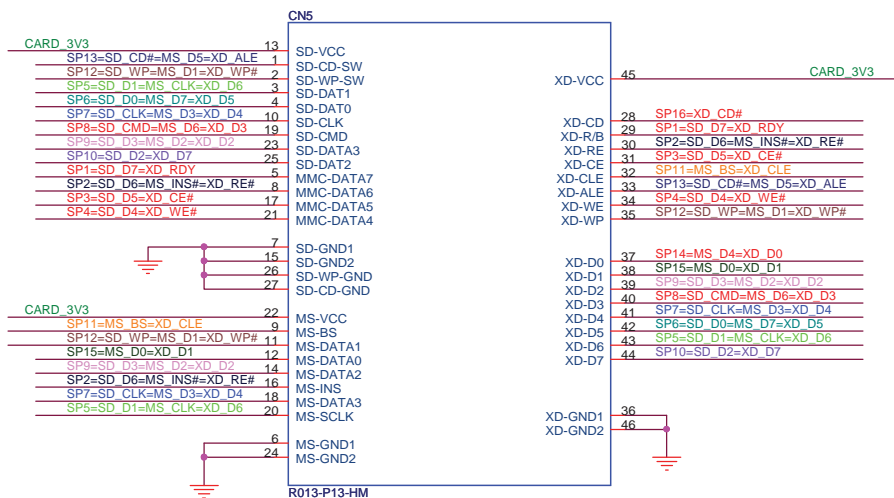
SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#



10/7 change 0 ohm

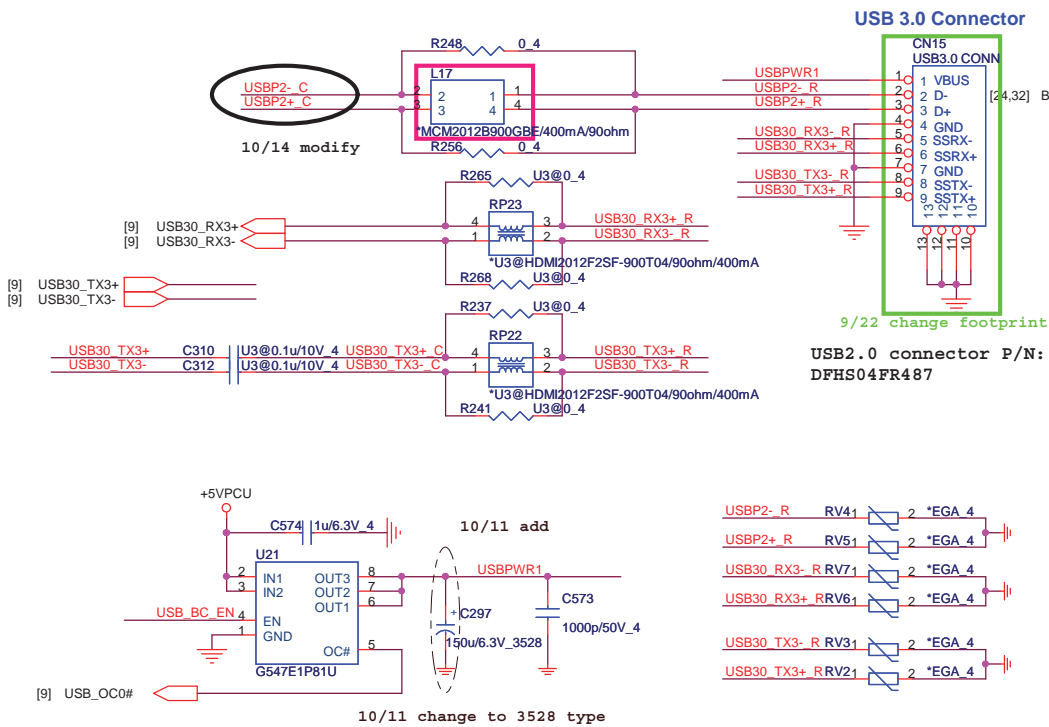


XD,MMC 4.2/SD,MS/MSP 7 IN1 CARD READER

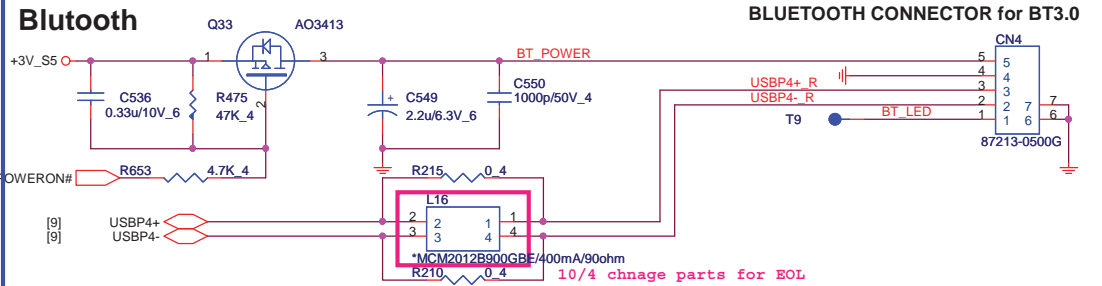


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PROJECT : ZQTA/ZQSA

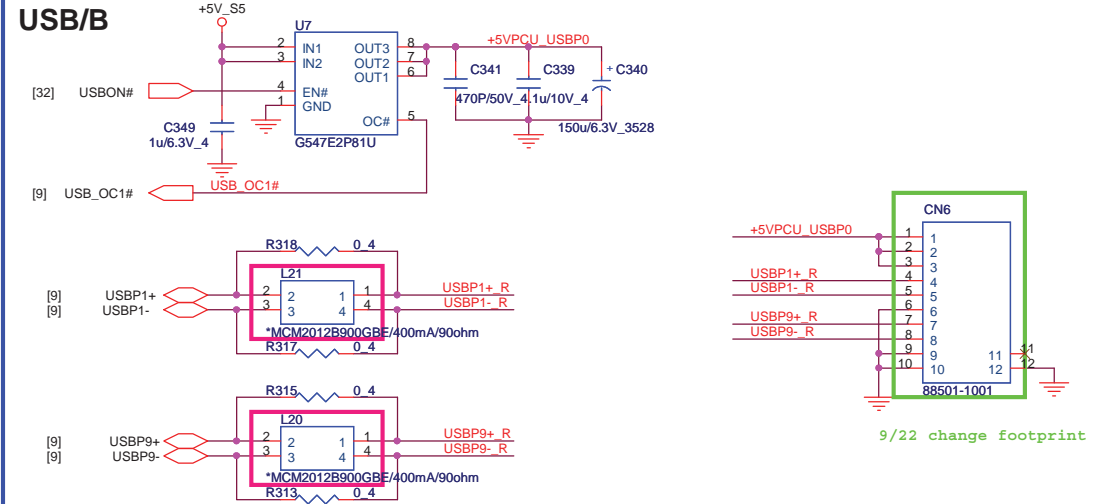
USB3.0/2.0



Bluetooth

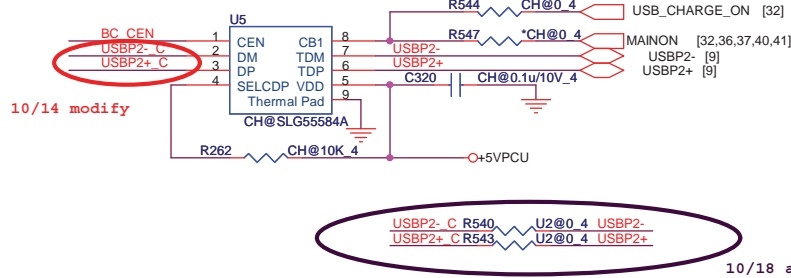


USB/B

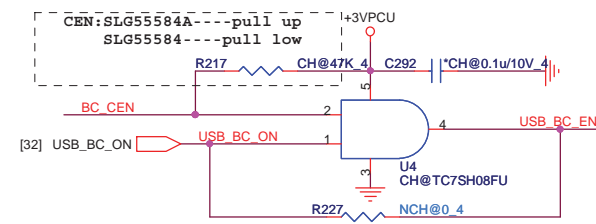


USB Charger to 3.0

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



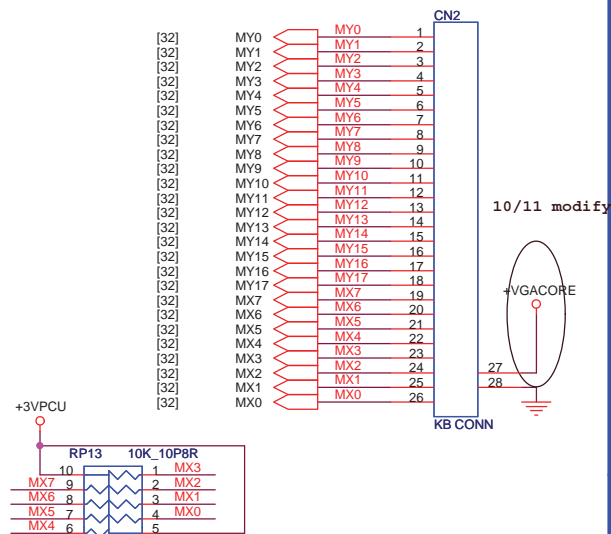
USB Charger -->CH@
None Charger--> NCH@



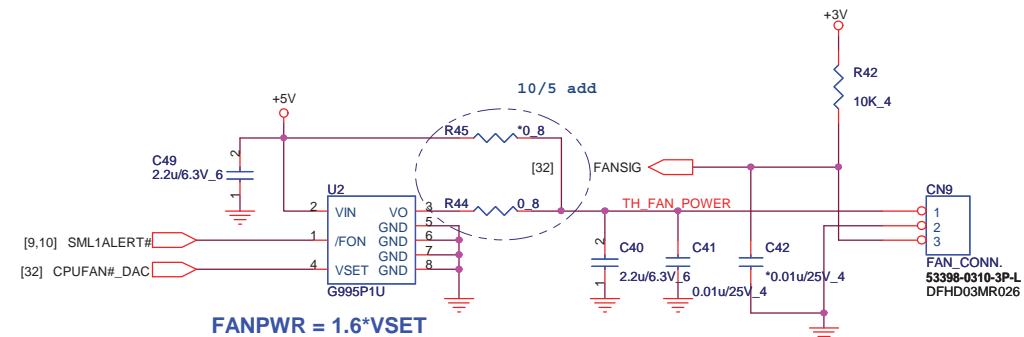
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size Document Number Rev 1A
USB/ BT/CHARGER
Date: Friday, November 11, 2011 Sheet 30 of 44

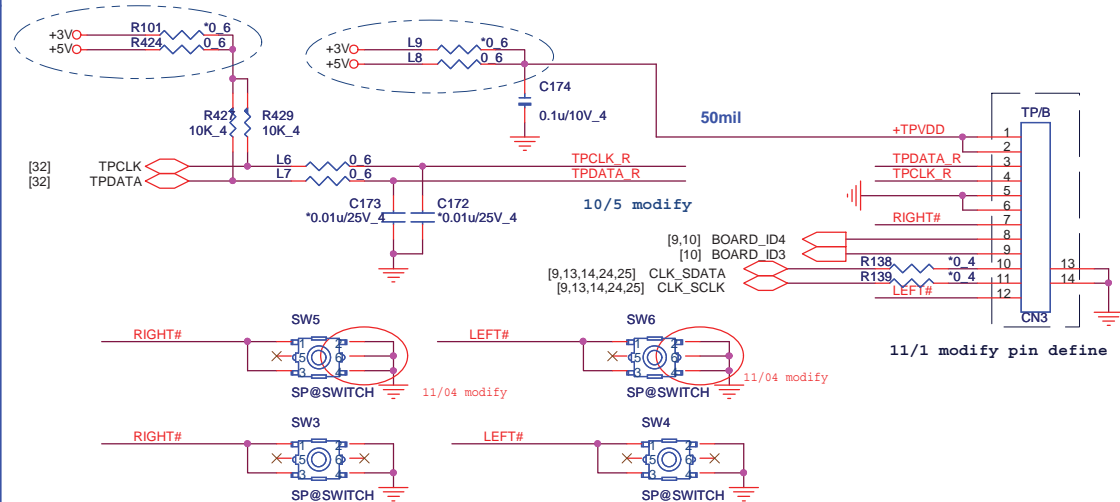
9/14 modify



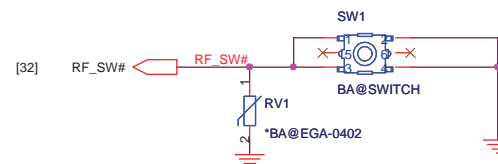
FANPWR = 1.6*VSET




```
Model EA/EG/BA---->SW3, SW4
      VA/VG----->SW5, SW6
```

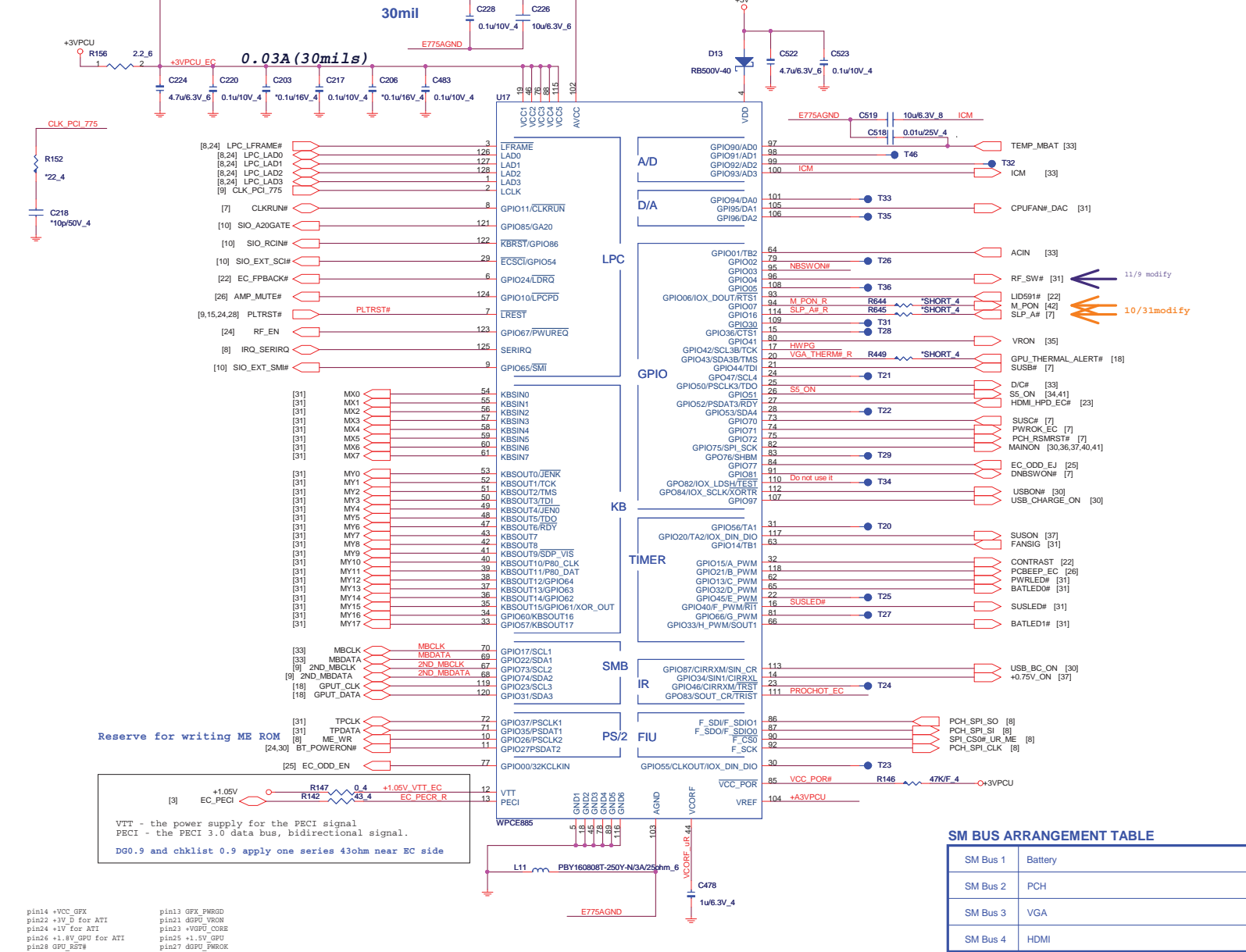


[32] RF SW#

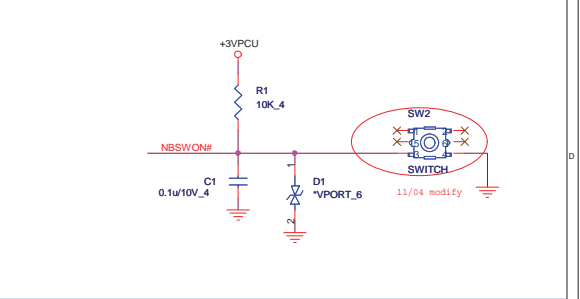


 Quanta Computer Inc. PROJECT : ZQTA/ZQSA		
Size	Document Number KB/FAN/TP+FP/LED	Rev 1A
Date:	Friday, November 11, 2011	Sheet 31 of 44

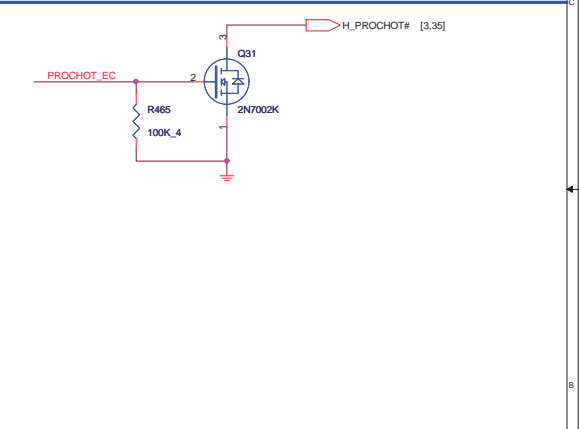
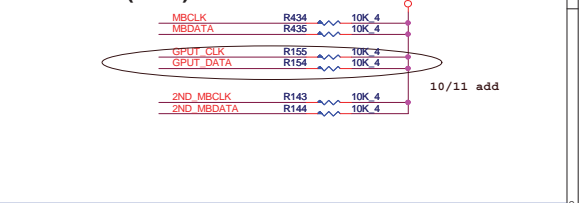
EC(KBC)



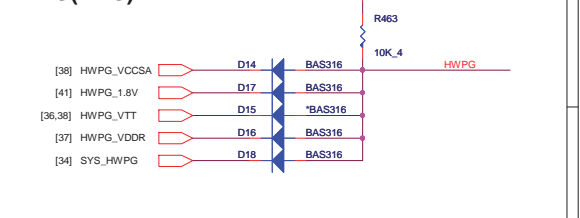
Power on bottom

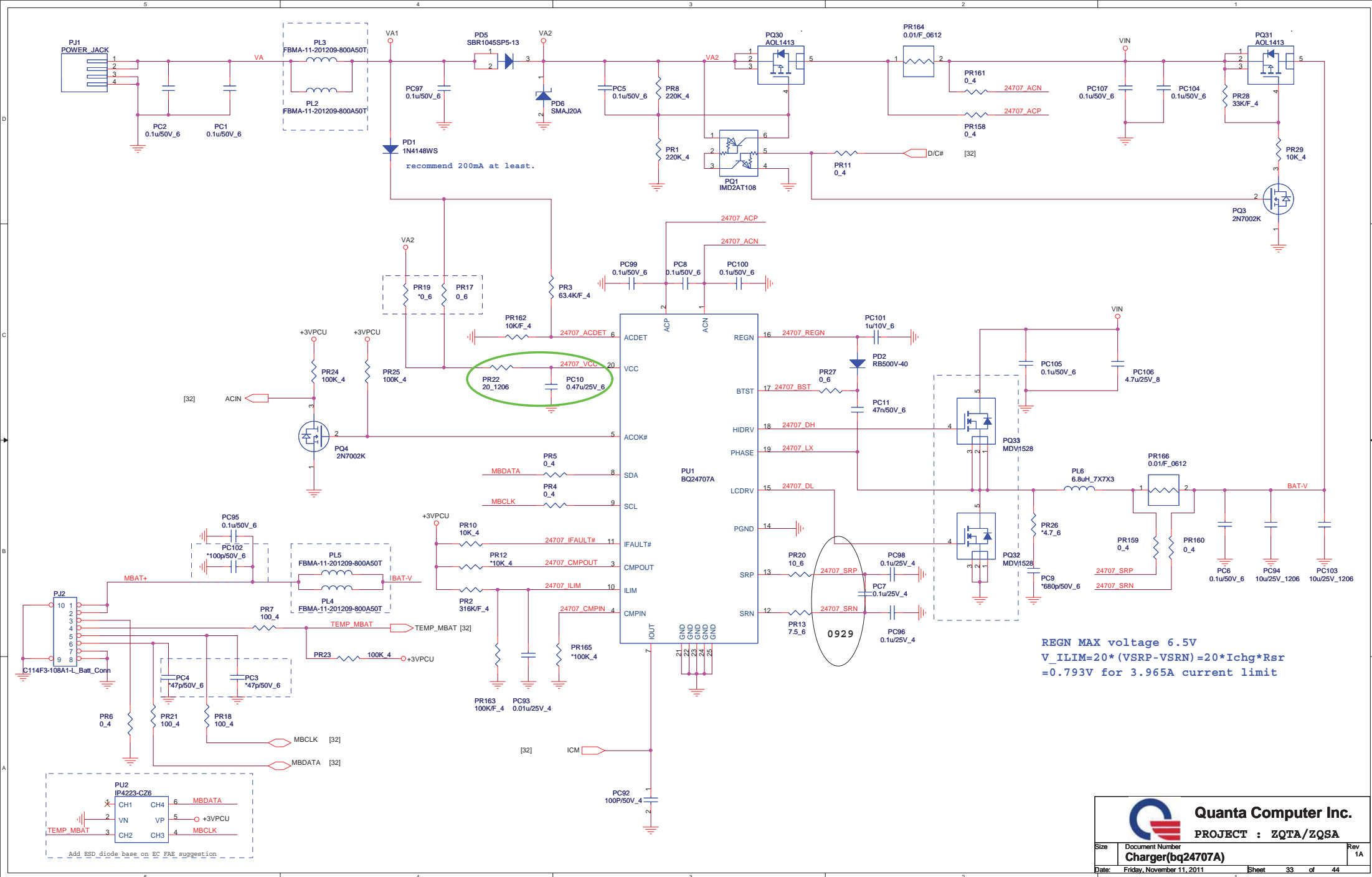


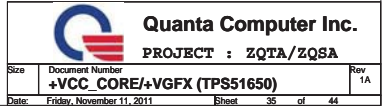
SM BUS PU(KBC)

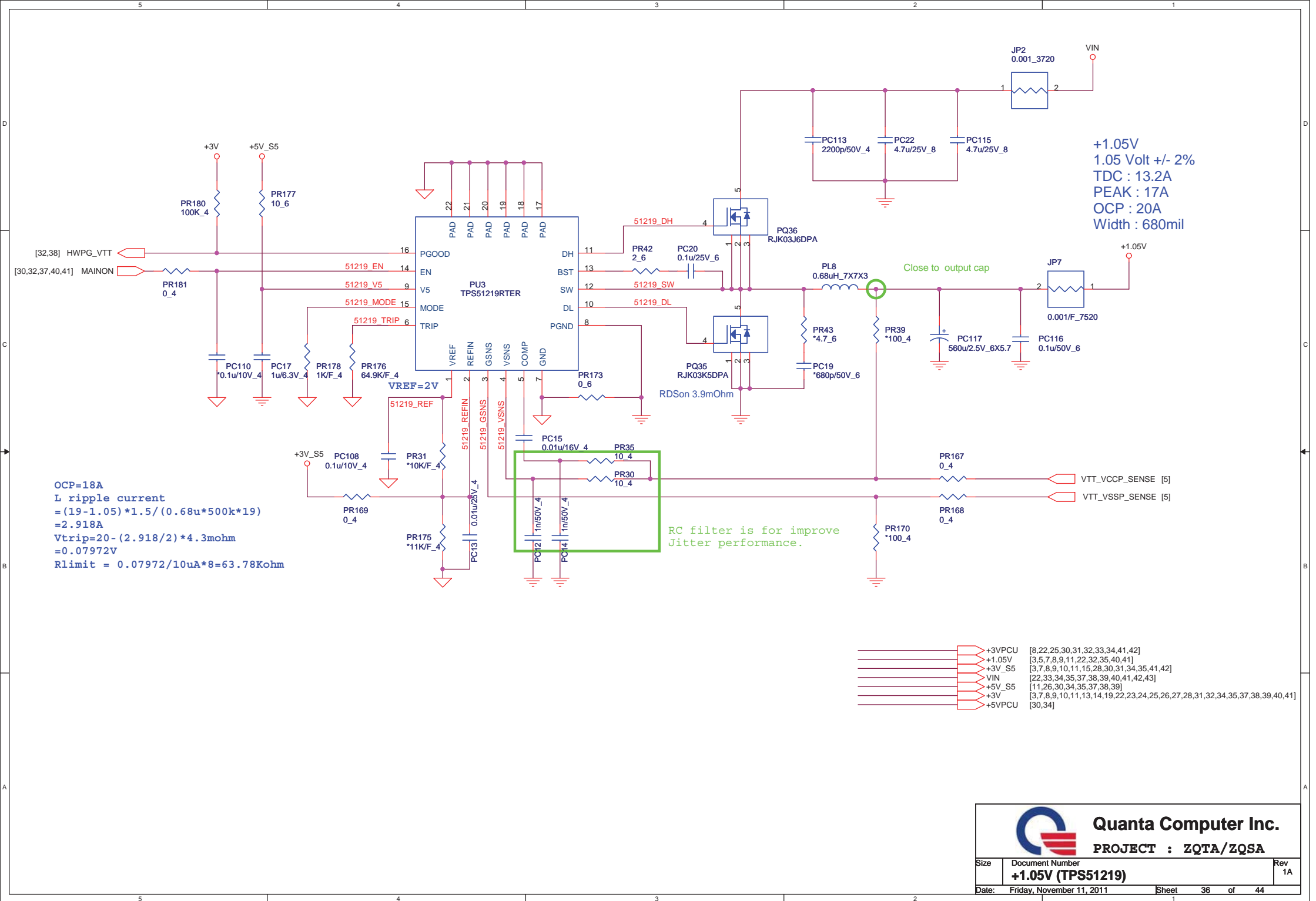


HWPG(KBC)







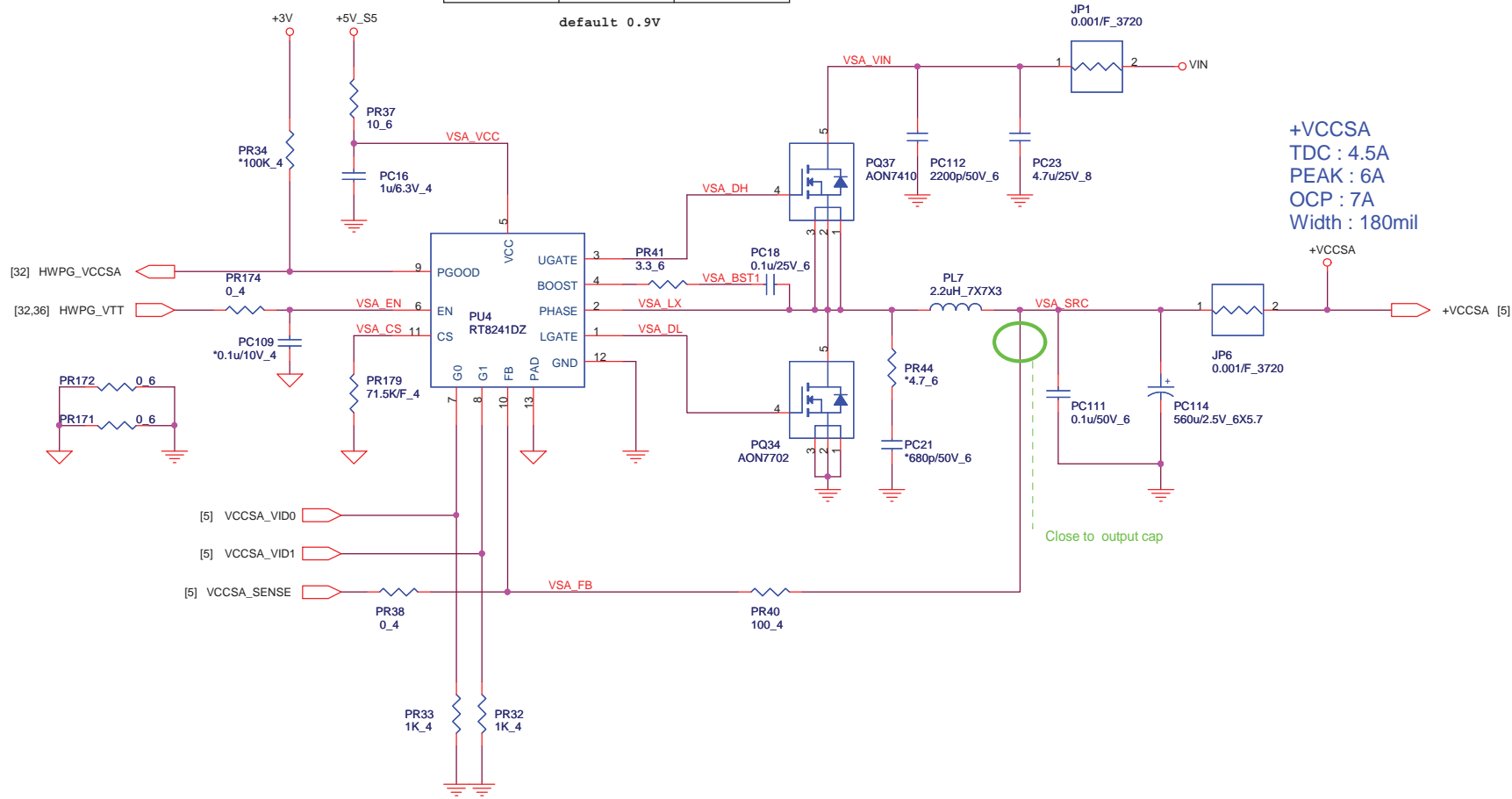


Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	+1.05V (TPS51219)	1A
Date:	Friday, November 11, 2011	Sheet 36 of 44

G0	G1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V



+VCCSA
TDC : 4.5A
PEAK : 6A
OCP : 7A
Width : 180mil

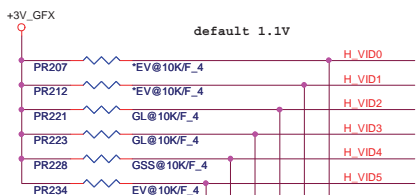
Close to output cap

OCP=7A
Iripple=(19-0.9)*0.9/(2.2u*300K*19)
=1.299A
Rth=14mohm*8*(7-0.65)/10uA
=71.125K
Ipeak=8.299A



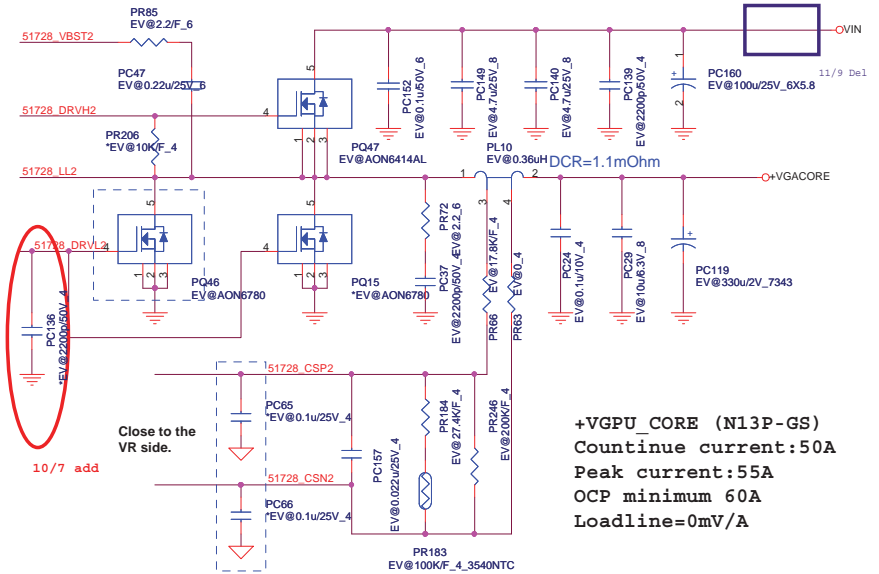
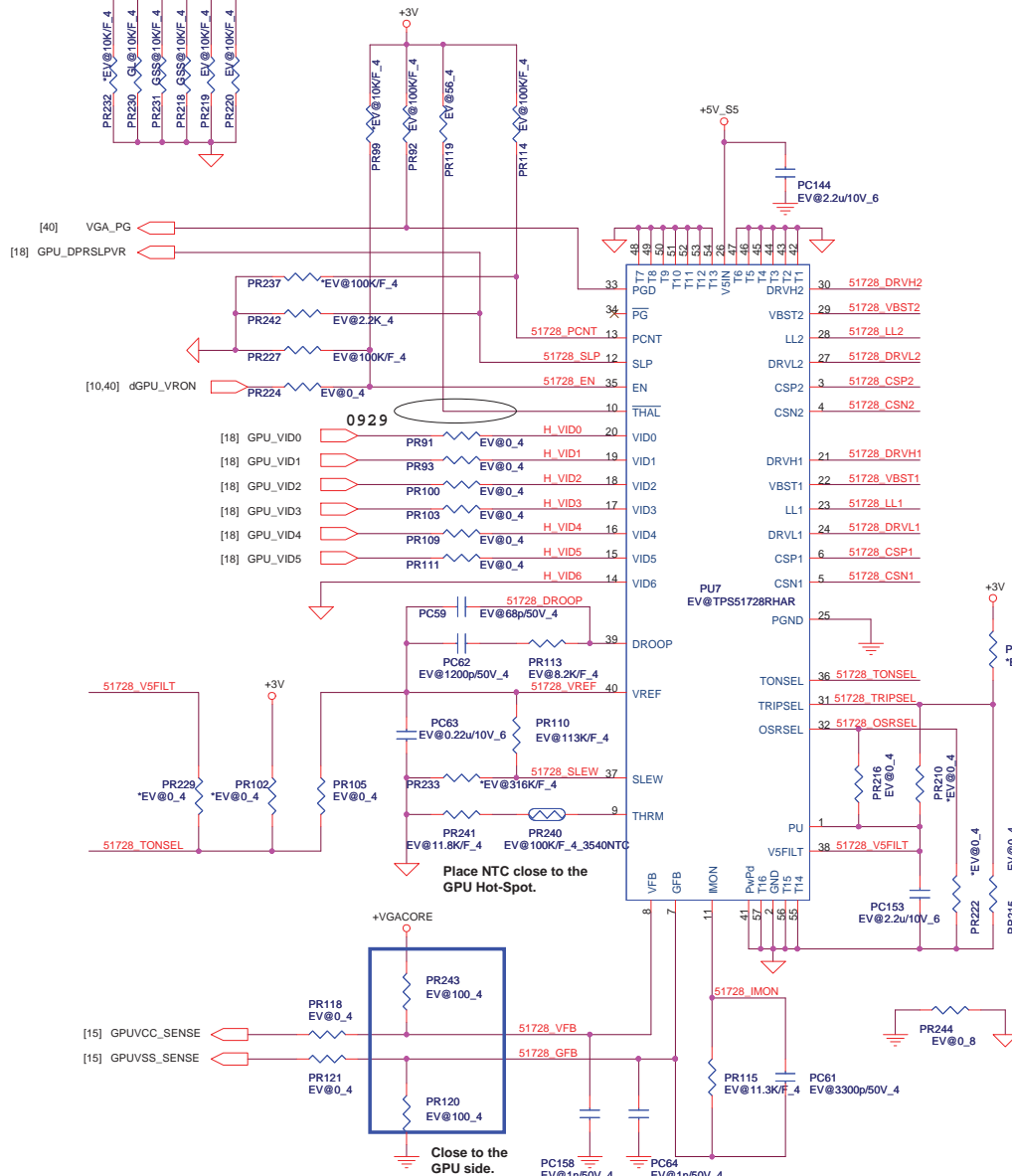
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	VCCSA(RT8241DZ)	1A
Date:	Friday, November 11, 2011	Sheet 38 of 44

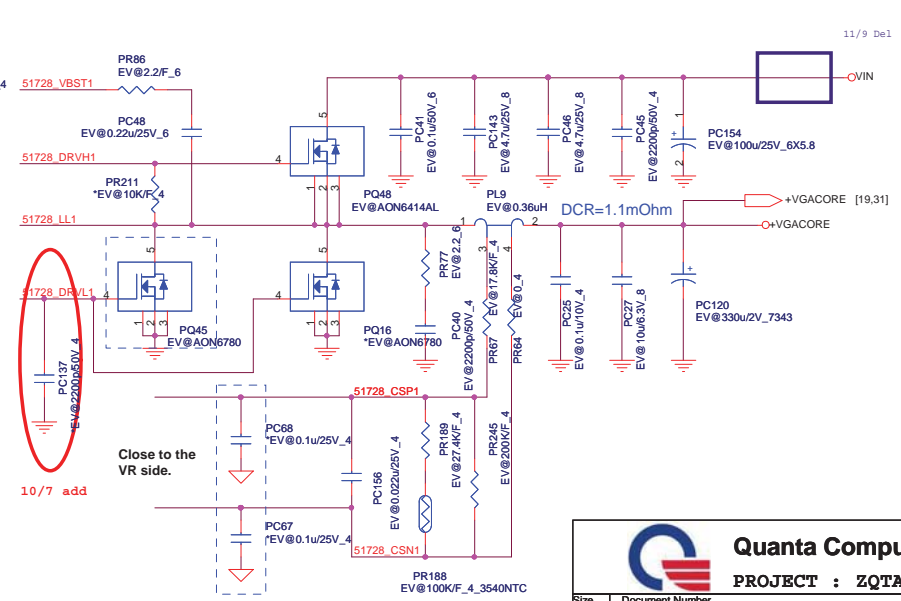


1013

	VID5	VID4	VID3	VID2	VID1	VID0
N13P-GL QS	1	0	1	1	0	0
N13P-GS QS	1	1	0	0	0	0
N13M-GS ES						



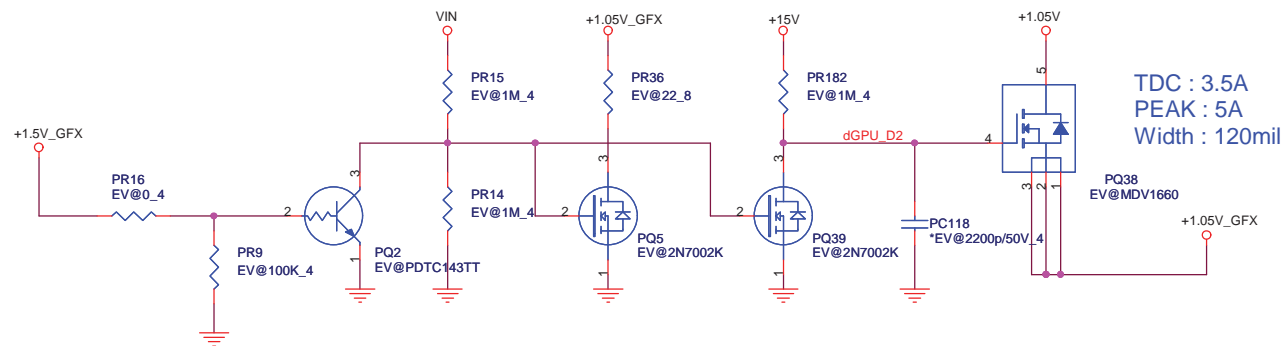
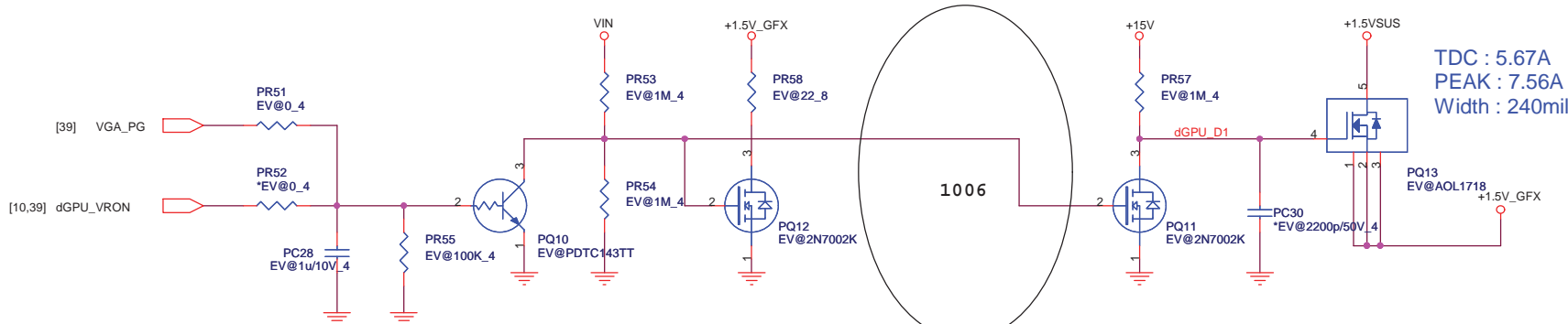
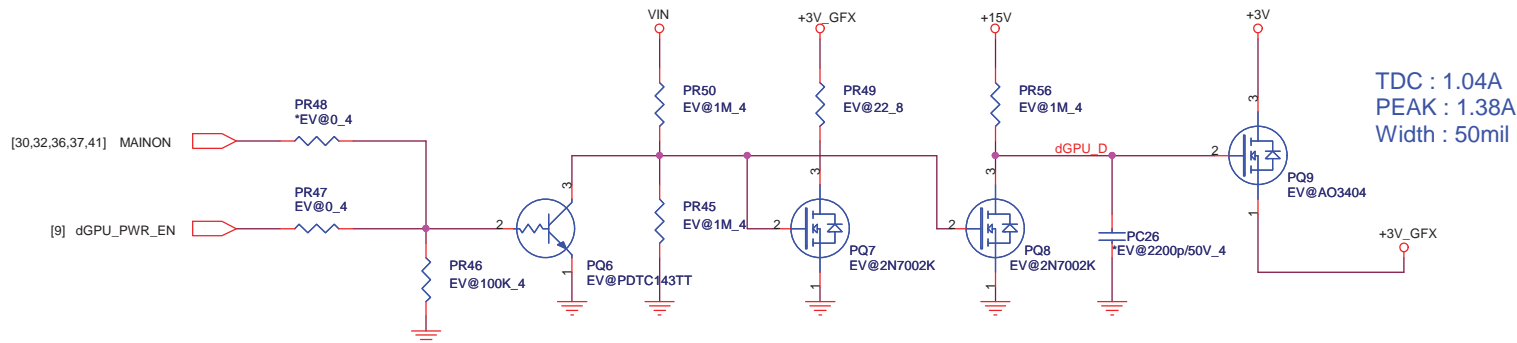
+VGPU_CORE (N13P-GS)
Continue current:50A
Peak current:55A
OCP minimum 60A
Loadline=0mV/A



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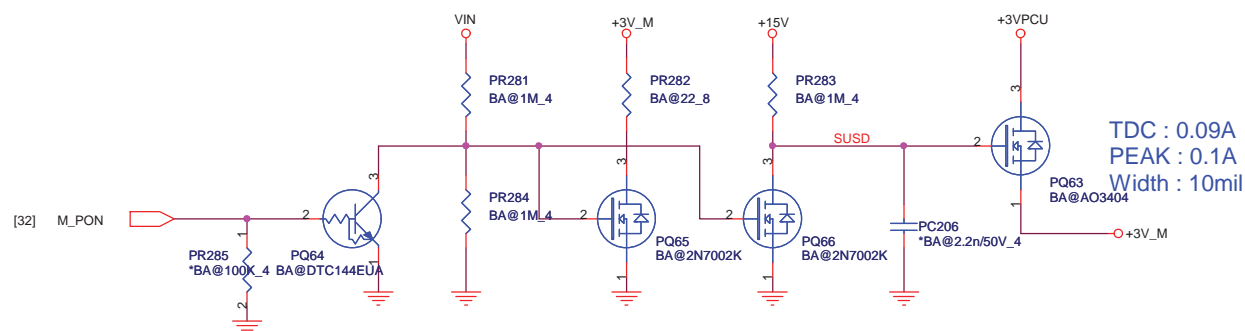
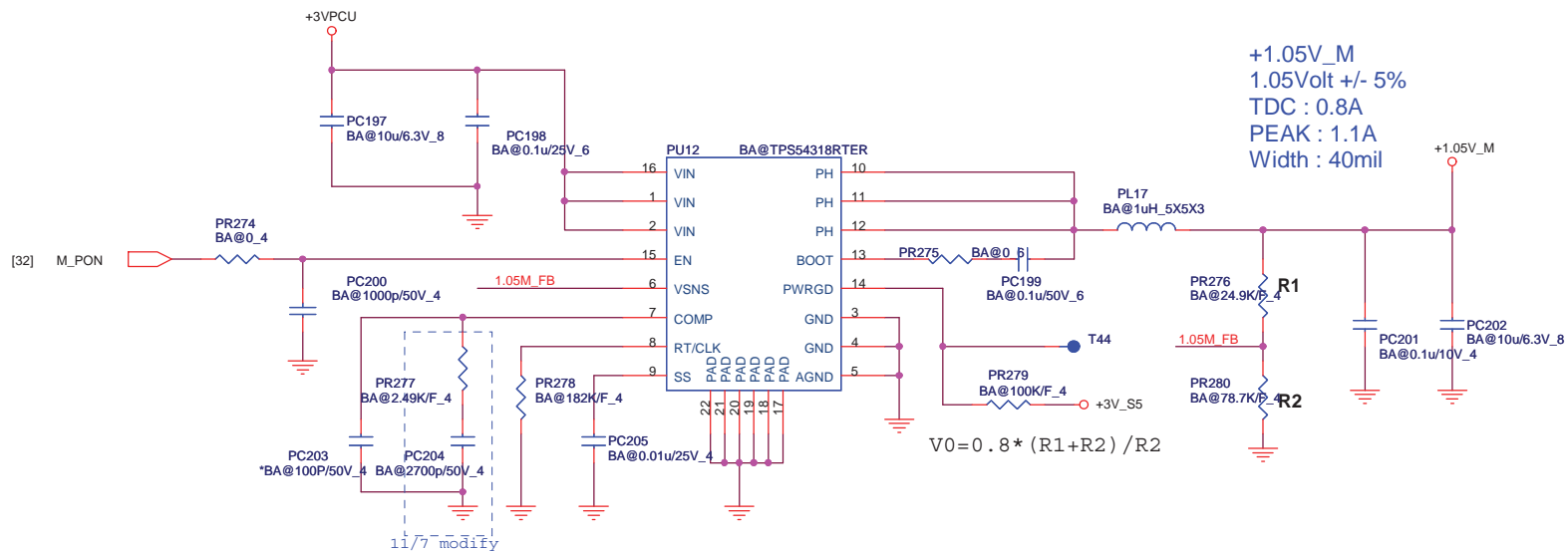
PROJECT : ZQTA/ZQSA

Size: Document Number
VGPU Core (TPS51728)
Date: Friday, November 11, 2011 Sheet 39 of 44 Rev 1A



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PROJECT : ZQTA/ZQSA

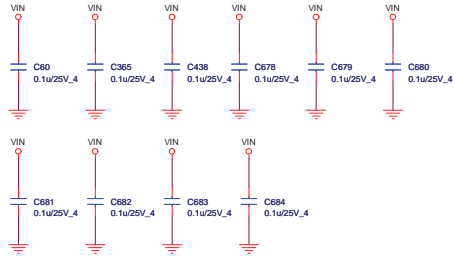
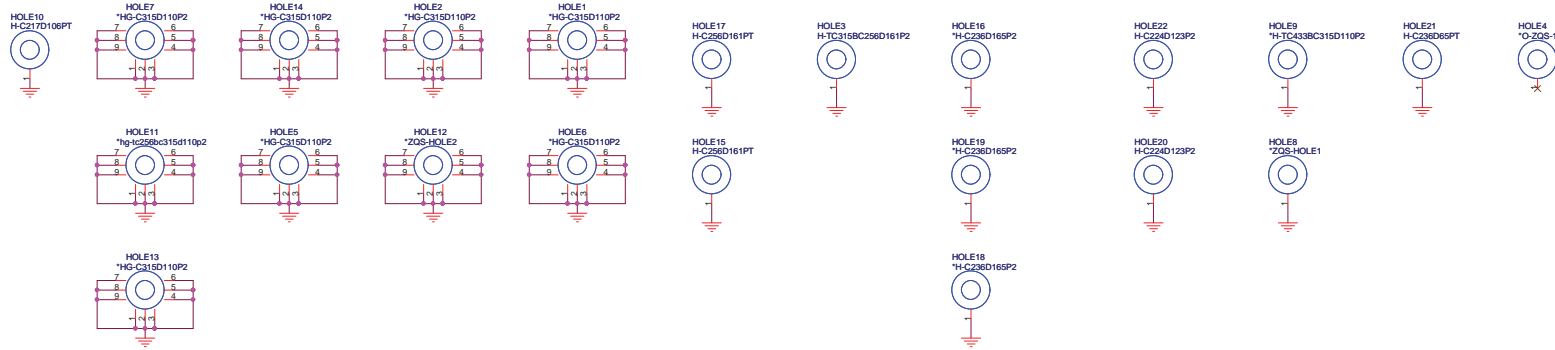
Size	Document Number	Rev
	GPU_PWR	1A
Date:	Friday, November 11, 2011	Sheet 40 of 44




Quanta Computer Inc.
 PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	+1.05V_M/+3V_M	1A
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Hole



Model	date	CHANGE LIST
ZASA/ZSQTA	9/26	page3 : add R511,R525,R527,R528,R529 for Discrete Only &PCH_JTAG_TDO net change pull-up from +3V_S5 to +1.05 rail
	9/27	Update power circuit Page19 : add C3777,C3778
	9/30	Page18 : add Q3508 for U7 GPU_THERMAL_ALERT net Page31 : Del CN1
	10/3	Page18 : add dGPU_ACDC# net to U7 GPIO04 & add R347 Page22 : add R557,R554 to pull-down & R548,R547 stuff for Discrete only Page25 : add R3693,C116 for ODD zero power circuit
	10/4	Page31 : CN8 add board id3 & board id4 net for touch pad ID control
	10/5	Page31 : CN8.2,CN8.3 add CLK_SDATA & CLK_SCLK net for touch pad & add R278,R279 Page15 : U41 Power rail change to +3V_GFX Page24 : Del Q16 no't support wake up function Page18 : add Q3509 for dGPU_ACDC# net Page31 : add L35,R3694,R3695 for touch pad 5V & 3V option & add R297,R295 Fan PWR option
	10/6	Page17 : IFPAB_PLLVDD rail change from +1.8V_GFX to +3V_GFX Page27 : U6 change footprint Page39 : PWR engineer add PQ3006,PQ3005 Page40 : PWR engineer Del PR193,PQ51,PQ54
	10/7	Page16 :add C3779,C3780 Page29 :add C542,C530 for EMI solution & C544 change to 4.7u 0603 type Page35 :PWR engineer add PC3037,PC3038,PC3039 Page35 :PWR engineer add PC3035,PC3036
	10/11	Page8 :add R376,R381,R393,R407,R421,R434 for Dual SPI ROM Page9 :U13 power rail change to +3V Page10 :SV_DET_NC net add R250 to pull-down Page27 :add R133,R235 Page30 :C443 change to 3528 type & add C366,R340 Page31 :CN2.27 pin change to +VGACORE Page32 :add R330,R328 pull-up +3VPCU for GPUT_CLK,GPUT_DATA net
	10/14	Page20 :add C3781,C3782,R3569,R3570,R3571,R3576 Page21 :add C3783,C3784,R3577,R3578,R3579,R3581

 Quanta Computer Inc. PROJECT : ZQTA/ZQSA		DOC NO.	PROJECT MODEL :	ZQTA/ZQSA	APPROVED BY:		DATE:
Size	Document Number		PART NUMBER:		DRAWING BY:		REVISION:
Change list Date: Friday, November 11, 2011		Sheet 44 of 44	Rev 1A				